

Fermilab - DES 12 Channel CCD Acquisition Board Test Procedures

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Revision History

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1.0 Introduction

This document covers the testing strategy for the FERMILAB-DES 12 CHANNEL CCD Acquisition Board to take the board from post-manufacture to a fully functional state. All tests described in this document pertain to the latest hardware revision level of the subject board. The test procedure assumes that the tester is familiar with the use of the MEC (MONSOON Engineering Console) and can execute the required commands. The tests are divided into progressive stages ranging from 1 to N. Each higher number stage uses assumptions on the board condition that requires the previous stages to have been successfully completed.

Stage 1. Preparation of Documentation

Stage 2. Board Finishing to ConFigure the Board to Meet Specifications

Stage 3. Mechanical Fit, Power Consumption and Firmware Programming Tests

Stage 4. Basic Bus Transactions and System Clock Tests

Stage 5. High Voltage Bias Tests

Stage 6. DOP Output Port and ADC Functional Testing

Stage 7. CDS Control Functions and Video Channel Performance Testing

Stage 8. Front-end Electronics Performance Analysis

In the description for these tests, certain conventions are followed to ease comprehension. These conventions and examples of each are presented in Table 1.

Table 1 - Test Description Conventions

Convention	Example	Description
Linux commands that are typed on a PAN xterm window	mecStart	Boldface characters
Commands typed to the MEC command line	<i>ppxSetAVP</i>	<i>Boldface italics</i>
Buttons on the DHE boards or MEC console	<u>>startExp<</u>	<i><u>Bold italics underlined</u></i> <i><u>inside > < symbols</u></i>
Designate data values that are returned in the PAN xterm or MEC console window	<i>dir</i>	<i>Italics</i>
Responses from the programs	this is a response	Courier font
Specific board signal names	FBIAS1	BOLDFACE SMALL CAPITALS
MEC attribute names	<i>mcbCodeID</i>	<i>Boldface italics</i>

The tester will record the result of each test in the MEC test record window. When the test results are saved, a file will be created called MNSN-EL-08-0500-SNnnn-xx.btr

(where MNSN-EL-08-0500 refers to the board production code, SNnnn is the serial number and xx is the test sequence number for this board. The file extension (.btr) stands for “Board Test Result”). This file should be saved on the local computer in a convenient directory, for example, DES 12 Channel Acquisition/BoardTests. At completion of testing, this file and the generated test report should be copied to the relevant area of the DES document archive:

(/MNSN/MonsoonAdmin/Production/TST_Repository/TSTResults/...).

This file is a record of the test and an analysis of the test results that can be printed out and kept in the system binder supplied to the end user. The test procedure functions will request the entry of data as required.

1.1 Required Equipment

- DHE with programmable power supplies and 6-slot backplane chassis.
- 12 Channel Transition module
- Fermilab Fanout board
- Personal Computer running MS Windows 2000 or Windows XP. The PC must be connected to the network with the \\decapod\MNSN disk mapped into the Windows disk structure. Required programs are MS Word and Xilinx Impact.
- JTAG-programming cable.
- Oscilloscope - Agilent 54622D or any of the Agilent 54600 series, a digital multimeter, and signal breakout box attached to the test transition board if fitted.

1.2 Test Schedule

Stage 1. Preparation of Documentation and Board Finishing to Configure the Board to Meet Specifications

Step i. If the board under test does not have a serial number, it is up to the user to place one on the board. Local directives will apply. See Figure 1 for serial number location.

Step ii. Create a new Assembly Record Tag (ART) for the board using the Word template. This document becomes the history of all work carried out on the board after manufacture. After the configuration and testing of the board, a printed copy should be made and attached to the circuit board protective box.

Step iii. Using a comparison photograph or a known good board, visually inspect the board for physical damage, missing and misplaced components. Figure 1 shows a typical CCD Acquisition Board. The particular board under test may not have exactly the same layout as pictured.

Step iv. Install the jumper configuration (JP 1 - JP14) according to the board configuration specification and make a note of their positions. Update the ART record with the jumper strapping information.

CCD Acquisition Board (Typical) [Figure 1](#)
Serial Number

Stage 2. Configure Board Firmware and Check Power Supplies

Step i. Locate a test backplane, a suitable power supply, and a PAN computer. Inspect the backplane for bent pins and fit 12 Channel Transition board to the rear of slot 6 and fit the test cables from the fanout board to the transition card. Set the power supply voltages and over-current limits to those listed in Table 6 in Appendix II

Step ii. Insert a known good Master Control Board (MCB) into slot 1. Connect the fibers to the PAN computer and power up the +3.3V and +5VD power supplies to the chassis.

NOTE: Slot 1 is marked with a triangle on the PCI back plane and normally has the board guide rails in a unique color.

Step iii. Open two xterm windows on the PAN. In the first xterm window, type fs0 and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the DHE to be in reset mode by having the *dir*(ection) bit true in the IO register (*i=01xx0*). The status command should return something similar to the following:

```
FibreXtreme (SL) Monitor (sl_mon) rev. 3.02 (2003/10/06)
Driver: rev. b2-835455:776764 for Linux with API rev. 2.1
Hardware: unit/bus/slot 0/1/4 - SL100 (D64) Firm. 1C.13 (1C.13) for
5.0V PCI
Link Control Register (CSR 0x08) = 0x37
Link Status Register (CSR 0x0c) = 0x200 Link is UP
FPDP Flags Register (CSR 0x10) = 0x200 NR.D.P2.P1.S: i=01110 o=00000
FIFO Threshold Register (CSR 0x14) = 0x0 Int.thr. = 0x0
Data count = 0xE75D (59229) bytes
```

```
Link (and other) Errors = 3
Configurable parameters:
Loop Configuration: 0 (Point-to-Point)
Max Timeout: 600000 (6000000 ms)
Flow Control: 0 (NO) Halt on link error: 1 (YES)
CRC generate/check: 1 (YES) Allow Queuing on link error:
```

Step iv. Use the command fc0 to clear the read buffer. Confirm with the status command that the read FIFO buffer is now empty (*Data count = 0x0 (0) bytes*) and that no link errors persist.

NOTE: Before proceeding with Step v, know what the PAN network name is and either create or identify an existing data directory in which to store the acquired data for test analysis. The PAN network name and the data directory name are then substituted in the command for the panMachineName and data variables.

Step v. In the second xterm window, start the PAN software and MONSOON Engineering Console using the command:
mecStart ccdBrdTest panMachineName /localFITS 65

The four PAN process windows and the MEC window should appear. See [Figure 2](#).

Initial MEC Screen
Figure 2

Step vi. Verify that the text fields “Step 1. Enter Host Name” and “Step 2. Port Number” contain the correct PAN machine name and port number (5142). Press the **>STEP 3. CONNECT<** button on the MEC. The Attribute Display pages will appear. Next press the **>RESET<** then the **>ASYNCRESP<** buttons on the MEC console. This achieves synchronization of the communication link. You should receive an OK: ppxAsyncResp: Success message in the MEC console message area and the “PIX” and “SEQ” LED’s on the MCB should have been extinguished. See [Figure 2](#). If the message is the same as that in [Figure 2](#), that is, ‘OK[SIM] :ppxAsyncResp:...’, then communication between the DHE and PAN has not been established. Follow the procedures in Appendix III to diagnose this problem. (Appendix III is missing . Please get Mark or Nick to elaborate on this – Since it never happens to me ☺)

MEC Screen after Connection, >reset> and >asyncResp>
Figure 3

Step vii. Press the >SYSTEM SETUP< button and execute "step 5." of the setup procedure. Open the **ENVIRONMENT** attribute screen in the Attribute categories window and press >UPDATE<. This loads the environment variables to the respective PAN attributes.

Step viii. Continue the configuration of the system by clicking on the Major Mode File Load button. This loads the appropriate mode file to the MCB.

Step ix. At the command entry box in the MEC, press the >LOAD BOARD TESTS< button. This will load the board test loader GUI frame into the MEC. Press the button marked >LOAD TEST FRAME< that corresponds to the type of board to be tested. Another frame should appear on the computer screen that contains specific tests for the board.

Step x. Enter the test technician's name into the appropriate entry box and check the date test date value.

Step xi. At this time, manually calculate the nominal power consumption of the MCB. Multiply the +3.3V and +5VD power supply voltage reading by the corresponding current consumption readings taken from the power supply. Add these two values together to arrive at a value in Watts for the MCB power consumption. Enter this value into the appropriate entry box on the test form.

Step xii. Leave the PAN software running. Power down the DHE chassis power supply.

Stage 3. Mechanical Fit, Power Consumption and Firmware Programming Tests

Step i. With the power to the chassis off, carefully insert the new board for the first time in slot 6. While inserting the board, check for the alignment of the connectors and front panel keying if fitted. Connect a JTAG programming cable to the JTAG port and the programming pod.

Step ii. Apply power to the DHE by switching on only the +3.3V and +5VD digital supplies.

Step iii. Enter the three-digit serial number of the board under test in the appropriate entry box of the test frame. The board serial number is found engraved on the front panel of the board.

Step iv. Initialize the IMPACT JTAG tool. Now follow the procedures outlined in Appendix I to load the field programmable devices. Annotate the firmware filenames and checksum information in the appropriate entry boxes in the test form and annotate these data to the ART record.

Step v. Power down the DHE, wait a second, and re-apply power to the DHE in the following order: the +3.3V and +5VD digital supplies first, then the +5VA supplies, then the +15VA supplies, and finally any +/-HV supplies. This order should be followed

whenever applying power to the DHE. To power down the DHE, the reverse order should be followed. This assures that the analog circuitry is always under control whenever power is applied or removed.

Step vi. The front panel LED devices on the MCB and the CCD Acquisition board should all be illuminated. Press the front panel >RESET< on the CCD Acquisition board. The front panel LED should extinguish and then illuminate again when the reset switch is released. This proves the FPGA boot circuitry is functioning. During a front panel reset operation, the firmware is reloaded to the FPGA from the EEPROM device.

Step vii. Compare the power supply consumption with that noted in Table 6 in Appendix II. Enter the power supply readings in the appropriate entry boxes in the test form from measurements taken from test points noted in [Figures 17 and 18](#).

Stage 4. Basic Bus Transactions and System Clock Tests

Step i. On the MEC , press the >RESET< then the >ASYNCRESP< buttons. The front panel LED devices on the MCB should extinguish.

Step ii. On the MEC configuration files window, press the >Sequencer Setup< and >Major Mode Load< buttons to reload the test mode file and sequencer program code to the boards. The front panel LED for the CCD Acquisition board should flash and extinguish. This proves the basic functioning of the board clock and sequencer bus operation.

Step iii. Press the button marked >Update Values< located on page 4 of the test form. The associated informational values from the CCD Acquisition board should appear in the entry boxes. Verify that these are rational values for the board. This proves the basic pixel bus functions.

Step iv. Repeatedly press the button marked >Toggle D5 LED< on page 4 of the test frame. Observe that the two LED devices physically located close to the CPLD devices turn on and off in relation to the button. This proves the basic functioning of the serial configuration bus of the CCD Acquisition board.

Stage 5. High Voltage Bias Tests

Step i. Set up the signal breakout box to access the HV Bias test points, a good quality DVM, and an oscilloscope set to 5v vertical deflection, 50ms / x division, and auto trigger. Alternatively, load the oscilloscope setup from the file **Agt54600_ccdBrdTestStep5i.sep**. On the test form Stage 5 page, click on the button marked >Set Bias Dacs 10%< on

Step 5i. All HV Bias voltages will be set to their 10% level. Measure each individual voltage to two decimal place precision on a DVM and enter these values into the entry boxes in the test form. Look at each HV Bias voltage with the oscilloscope to detect any obvious oscillations or ringing behavior.

Step ii. While the HV bias voltages are at the 10% level, press the button marked **>Read Telemetry<** for Step ii. This will invoke a measurement of all HV Bias voltages via the telemetry circuits of the board. These measurements will be displayed in the entry boxes associated with the test form. Observe each individual measurement within the four groups to determine if the values appear real. The variation of each reading within a group should not greater than 4 or 5.

Step iii. Click on the button marked **>Set Bias Dacs 50%<** on step 5iii. All HV Bias voltages will be set to their 50% level. Measure each individual voltage to two decimal place precision on a DVM and enter these value into the entry boxes provided on the test form. Look at each HV Bias voltage with the scope to detect any obvious oscillations or ringing behavior.

Step iv. While the HV bias voltages are at the 50% level, press the button marked **>Read Telemetry<** for Step iv. This will invoke another measurement of all HV Bias voltages via the telemetry circuits of the board. These measurements will be displayed in the entry boxes associated with the test form. Observe each individual measurement within the four groups to determine if the values appear real. The variation of each reading within a group should not greater than 4 or 5.

Step v. Click on the button marked **>Set Bias Dacs 90%<** on step 5v. All HV Bias voltages will be set to their 90% level. Measure each individual voltage to two decimal place precision on a DVM and enter these value into the entry boxes provided on the test form. Look at each HV Bias voltage with the scope to detect any obvious oscillations or ringing behavior.

Step vi. While the HV bias voltages are at the 95% level, press the button marked **>Read Telemetry<** for Step vi. This will invoke another measurement of all HV Bias voltages via the telemetry circuits of the board. These measurements will be displayed in the entry boxes associated with the test form. Observe each individual measurement within the four groups to determine if the values appear real. The variation of each reading within a group should not greater than 4 or 5.

Step viii. Click on the button marked **>Calc DAC Slopes<** for Step viii to compute the slope and intercept values from the means calculated in the previous step. These values should be used as calibration constants for the board description file. Process under investigation.

Step xi At this point the HV Biases are at their 90% full scale value. If the board has been con**Figure**d for negative HV Bias voltages, press the button marked **>Set Bias Dacs 10%<** associated with Step 5i to set the biases to their maximum negative voltage. Connect the scope to each individual HV bias test point while repeatedly pressing the button marked **>Disable HV DACs<** associated with this step. Each HV Bias should show a sharp return to AGND as they are disabled and an equally sharp return to their

level when enabled. This tests the ability to isolate the HV biases from a detector. While the biases are enabled, reset the vertical sensitivity of the scope to 5mv / division, AC coupled, and 20MHz bandwidth limiting. Measure the peak to peak noise values of each individual bias and annotate in the associated entry boxes of the test form. After all biases have been tested, leave the button in the green condition with the biases enabled for the next test.

Step xii Set the oscilloscope back to 5v division, DC coupled, 100ms horizontal deflection, normal trigger and a trigger level just below the maximum bias supply voltage. Alternatively, load the oscilloscope with the setup pattern from the file **Agt54600_ccdBrdTestStep5xii.scp**.

NOTE: This depends on whether the board is configured for positive or negative bias generation. Click on the button marked **>Toggle HV DACs<** associated with this test and adjust the scope to capture the positive going edge of the HV Bias signal. Measure the rise time for each individual bias and annotate this value into the entry boxes. Make sure that the negative edge is also within the same range as the positive transition. These edges will be different from board to board due to configuration options but should be approximately 65 milliseconds rise and fall.

This completes testing of the HV bias generators and HV bias telemetry circuits.

Stage 6. DOP Output Port and ADC Functional Testing

Step i. Click on the button marked **>Run DOP Bit Test<** and monitor the values that appear in the two entry boxes of the test form. The write value is the one sent to the port, the read value is that which is read back from the board register. Correct correspondence of these values proves the ability of the board to accept 32-bit data (Sequencer bus) and to drive 32 bits to the master control board. When this has been verified, stop the test by pressing the button again.

Step ii. Click on the button marked **>Run DOP Block Test<** to further verify the writing ability of the DOP port. As before, check the correspondence of the data values in the GUI entry boxes and the correct code on the DOP interface connector. This test does a reasonable job of detecting stuck or crossed over bits.

Step iii. Click on the button marked **>Calc ADC Offsets<** for this step. The video channel ADC devices are triggered and readings obtained while the video offset DACs are set to 10%, 50% and 90% of their dynamic range. The ADC readings are used to calculate the slope and intercept of the DAC range in units of ADU. The mean data values returned in the entry boxes should be within 100 ADU of each other and the slope value reasonably consistent.

Step iv. Click on the button marked **>Set ADC Baseline<** for step iv. The offset values to reach 10,000 ADU are set to the ADC offset DACs and a series of readings taken from the ADC. The MEAN readings should be close to the set point (10,000 ADU) and the

standard deviation below 3 ADU. It may take several attempts, that is, repeated pressing of the button, to reach the low value of standard deviation.

Stage 7. CDS Control Functions and Video Channel Performance Testing.

Step i. Connect the oscilloscope to the CCD Acquisition board using [Figure 4](#) and Table 2 as a guide. Connect the oscilloscope to a suitable computer, establish communication with the oscilloscope and download the setup file using the Agilent Excel or Word tool bar add-ins. The setup file is called **Agt54600_ccdBrdTestStep7i.scp**.

CCD Acquisition Board Test Points [Figure 4](#)

Table 2 - Agilent Oscilloscope Logic Analyzer Connections

Agilent Oscilloscope Logic Analyzer Pods

Pod 1

Pod 2

D0 => U60 FTP1

D8 => U60 FTP9

D1 => U60 FTP2

D9 => U60 FTP10

D2 => U60 FTP3

D10 => U60 FTP18

D3 => U60 FTP4

D11

D4 => U60 FTP5

D12

D5 => U60 FTP6

D13

D6 => U60 FTP7

D14

D7 => U60 FTP8

D15

Gnd => DGND

Gnd => DGND

PIN 3 PIN 5 PIN 7 PIN 9 PIN 11 PIN 13 PIN 15 PIN 17 PIN 1 200K OHM AGND SIGS STIM SHUNT PLUG P4

Shunt Plug Jumper Configuration [Figure 5](#)

Using [Figure 5](#) as a guide, install a short jumper cable between AGND and the SIGS connections on the shunt plug. Install this plug on the video channel input connector (P4) of the CCD Acquisition Transition Board.

Step ii. In the test frame window, press the button marked *>Acquire an Image<*. This will initiate an acquisition cycle and result in a file being written to the data directory. This setup will acquire data from the ADC channels while the CDS circuit is held static. This test verifies the correct operation of the ADC devices and measures the noise of the circuit up to the DC Clamp switch in a static state. The oscilloscope will trigger and display a captured waveform similar to that shown in [Figure 6](#).

Waveform from Step ii [Figure 6](#)

Signals FTP1 => FTP5 are held on. FTP9 is the CTC (Command To Convert) pulse that triggers the ADCs. FTP6 shows the ADC response to this convert command by going busy for approx 800ns. After the conversion, FTP7 goes true (low) to indicate to the CPLD to transfer data to the FPGA. This is shown in FTP8, which is the CPLD => FPGA data bus enable signal for U60. During this time, two 36-bit bus transactions are made 25ns apart to transfer the four 18-bit results from the respective ADCs. FTP10

demonstrates the load pulses coming from the FPGA to the CPLD CDS latches and coincides with each edge of the CDS waveforms. FTP11 is used only to trigger the oscilloscope and coincides with the beginning of each separate pixel CDS process time. The acquisition process should finish without error and the filename of the acquired image appear in the entry box associated with this step.

Step iii. Press the button marked >Acquire an Image< in Step iii to acquire another file. This time the gain stage, phase inverter and integrator are run in a normal fashion while still holding the DC Clamp switch on. In this way the dynamic noise of the circuit can be measured up to the input of the gain stage (without the pre-amp). The scope will capture another waveform that should look similar to [Figure 7](#).

Waveform from Step iii [Figure 7](#)

This waveforms capture shows that the inverted / non-inverted phase switching of the signal is taking place on FTP2 and FTP1 respectively. The integrator is integrating during the time when FTP3 is true (high), and the integrator is taken out of reset when FTP5 is false (low). Note that the DC Restore signal (FTP4) is still held on. The acquisition process should finish without error and the filename of the acquired image appear in the entry box associated with this step

Step iv. Press the button marked >Acquire an Image< in Step iv to acquire another file. This time the DC Restore signal is released and a normal acquisition cycle is demonstrated. The waveform should look similar to [Figure 8](#).

Waveform from Step iv [Figure 8](#)

In the captured waveform in [Figure 8](#), the DC Restore signal is shown toggling off for the complete pixel process time on FTP4. The acquisition process should finish without error and the filename of the acquired image appear in the entry box associated with this step.

Step v. Press the button marked >Acquire an Image< in Step v to acquire another file. This time the electronic gain is switched into hi-gain mode. The captured waveform should look exactly like the previous acquisition ([Figure 8](#)). The acquisition process should finish without error and the filename of the acquired image appear in the entry box associated with this step.

Step vi. Press the button marked >Acquire an Image< in Step vi to acquire another file. This time the acquisition rate is increased by reducing the settling time between signal transitions and reducing the actual integration time of the integrator. The captured waveform should be similar to [Figure 9](#).

Waveform from Step vi [Figure 9](#)

Note the decrease in settling time between all CDS edges and the decrease in integration time shown by FTP3. At this point the CDS control functions are functional. The data

files produced by these tests will be used in Stage 8 to verify the functionality and performance of the CDS signal processing functions.

Step vii. Press the button marked **>Acquire an Image<** in Step vii to acquire another file. This data file will be used later to verify the offset DAC stability.

Step viii. Remove the jumper between AGND and the SIGS connections on the shunt plug installed on the video channel input connector (P4). Connect a jumper between the DOP port connector (P2) pin 34 and the shunt plug STIM connection. Connect the oscilloscope analog channel 1 to the front panel signal monitor jack P2. Connect the analog channel 2 input to test point TP51. Download the scope setup file **Agt54600_ccdBrdTestStep7viii.scp** using the Agilent Excel or Word tool bar add-in tool bars.

Step ix. Press the button marked **>Test CDS Signals<** and observe the waveforms acquired on the oscilloscope. Move the oscilloscope probes to each of the channels and compare the waveforms to that shown in [Figure 10](#). After confirming the operation of the analog signal through the CDS processing circuitry, press the button again to stop the test and remove all oscilloscope probes from the board.

Waveform from Step ix [Figure 10](#)

FTP1, 2, 3, 4 and 11 are showing the same signals. ANL_1 shows the output of the preamp for video channel 1. Signal ANL_2 shows the integrator ramp responding to the difference between the inverting integration level of the input signal and the non-inverting integration level of the signal.

Step x. Press the button marked **>Acquire an Image<** to acquire another file. This test uses the DOP port to simulate the negative-going transition of a CCD output transistor when pixel charge is dumped onto the CCD sense node. In this way the CDS signal processor is stimulated with a step function to assure that the gain is present and that the amplifiers are stable.

Stage 8 Front-end Electronics Performance Analysis.

Step i. Obtain a computer that has both IDL loaded/accessible and access to the data file directory where the files that were acquired in Step 7 are kept.

Step ii. If the computer to be used for testing has never been used to analyze MONSOON data before, use the command **mkdir /home/monsoon/IDL_WORK/ccdBrdTest** to create a directory for the IDL procedure source code. Load the IDL procedure source files into this directory. The file list of the IDL procedures is shown in Appendix III.

Step iii. In an xterm window, use the command **cd (directory name)** to change the directory to where the files created in Step 7 are stored. Start IDL by using the command **IDL**; an IDL prompt should appear. Use the command **!PATH =**

‘/home/monsoon/IDL_WORK/ccdBrdTest:’ + !PATH to establish a path to the analysis procedures. Compile the data analysis procedure by typing **run ccdBrdTest** at the IDL prompt. Note the full stop before the “run” command.

Step iv. For each of the following steps, initiate the analysis by invoking the IDL analysis procedure using the command **ccdBrdTest** in the IDL window. The procedure will present a file selection dialog where the pixel data file to be analyzed can be selected. The procedure then finds all appropriate FITS extensions in that file. Answer the following three questions to allow the procedure to analyze the file and report on mean, max, min, and standard deviation of the pixel data and plot histogram and row values.

- The first question is the number of sub-regions in the x (column) dimension. This value is usually 1.
- The procedure then asks for the number of sub regions in y (row) dimension. With one exception, the file created in Step vii, the response is usually 1. For Step vii, the answer is the value set in the attribute “Span” and is normally 16.
- The last question asks for a directory name in which to put the output results. This is a directory name relative to the data directory where the pixel data file is and will be created by the analysis procedure. It is suggested that each tested board use a single unique output products directory.

Step v. Run the analysis procedure and select the first file written by Step 7ii. The name of this file can be found by looking at the test form for that setup. This tests the basic ADC conversion function and offset noise values. All CDS switches are held static. The results should show an rms noise level below 3 ADU. Annotate the results of each channel’s mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step vi. Run the analysis procedure and select the second file written by Step 7iii. This test analyzes the noise component of all front end electronics up to the DC Clamp switch. The results should show less than 6 ADU rms noise for all channels. Annotate the results of each channel’s mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step vii. Run the analysis procedure and select the third file written by Step 7iv. This test allows the preamplifier noise to contribute to the overall noise [Figure](#). The inputs to the preamplifier should be shunted to ground with the shunt plug that emulates the expected detector output transistor impedance. Results should be less than 7 ADU rms for each channel. Annotate the results of each channel’s mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step viii. Run the analysis procedure and select the fourth file written by Step 7v. This test runs the front-end electronics in high gain mode to show what the noise distribution is. Noise from the preamp and gain stage will be amplified by the electronic gain. Phase inverter, integrator and diff buffer noise gain will stay the same. Results should show less than 10 ADU rms for each channel. Annotate the results of each channel’s mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step ix. Run the analysis procedure and select the fifth file written by Step 7vi. This test runs the front-end electronics at low gain and at 800 KPixel/second/channel if possible. Results should show a slight increase in noise from setup 03. Annotate the results of each channel's mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step x. Run the analysis procedure and select the sixth file written by Step 7vii This test uses the offset DACs as a ramp generator to test dynamic range of the ADCs plus stability and noise of the offset voltage. Plots should show consistent data spreads and no oscillation of levels. Use the value of 1 for the column sub-region prompt and a value of 16 for the row sub-region prompt. Annotate the results of each sub-region for each channel's mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step xi. Run the analysis procedure and select the seventh file written by Step 7x. This test uses the DOP port to simulate a ccd output level. Annotate the results of each channel's mean, standard deviation, maximum and minimum values to the spreadsheet in the appropriate section.

Step xii. The results of the performed tests are available for hardcopy review by loading the appropriate .html document from the previously defined output directory. The file name is the same as the original data file with the appropriate suffix appended. These documents can be copied and used to accompany the board as a 'proof of test' document to users of the hardware.

NOTE: The board can now be considered fully functional. Make sure that the filename for the **TEST SHEET** correctly reflects the product code and serial number of the board and store it in the **\\decapod\MonsoonAdmin\Production\TST_Repository\TestResults** directory. Make an Acrobat .pdf copy of the same file and store it in the **\\decapod\MonsoonAdmin\Production\HIST_Repository** directory.
Info to come from Nick B.

2.0 Appendix

JTAG usage and Field Programmable Device (FPD) setup.

2.1 Appendix I CCD Acquisition Board FPD Programming

Step i. Connect the JTAG cable to the JTAG connector on the CCD Acquisition board. With power applied to the board, check that the status LED on the programming pod shows green. If not, the JTAG plug may be reversed. The +3.3V signal line for the JTAG socket is the one closest to the reset button. When the pod LED shows green, initialize the JTAG chain with the Xilinx IMPACT program.

Step ii. Follow the default prompts to launch the tool in its configuration mode. You may need to right click the mouse and select ‘initialize chain’ to connect to the CCD Acquisition board JTAG chain. After initialization two devices should be present on the JTAG chain. [Figure 7](http://toolbox.xilinx.com/docsan/xilinx4/pdf/docs/pac/pac.pdf) shows a representative view. Further information on this tool can be found at: <http://toolbox.xilinx.com/docsan/xilinx4/pdf/docs/pac/pac.pdf>

Step iii. The Xilinx IMPACT application will ask you to select the appropriate files for each of the 2 devices. Use Table 3 to identify the correct load files. These files should be available from the local computer. If the IMPACT tool does not present a file menu to select the ‘File’ menu and click ‘initialize chain’ to accomplish this part.

Step iv. Place the mouse cursor over the first device icon (18V02) and right click. Select ‘Program’ and accept the default conditions (Erase before programming and Verify after programming). The tool will program the EEPROM device.

Step vi. If the board has not been programmed previously, power the complete board off and power on again to load the EEPROM boot contents to the Virtex device. If the board has been programmed previously, the front panel reset button can be used to re-boot the Virtex device. Once the board has re-booted, right click on the second device icon (XC300E) and select **verify**. The verify cycle should complete without errors.

Step vii. The respective device checksums and user codes can be recovered from the devices by using the correct menu item after right clicking the respective device icon.

Step viii. Close the IMPACT tool application and disconnect the JTAG cable.

Table 3 - CCD Acquisition Board - JTAG Device Description and Load Files

2.2 Appendix II. CCD Acquisition Board Power Supply Requirements

These tables outline the power consumption for a correctly operating board alone in a MONSOON chassis under test conditions:

2.2.1 Before Programming Power Consumption Tables

Table 4 - Power Supply Requirements (before programming)

Supply Name

Set Voltage

2.2.2 After Programming Power Consumption Tables

Table 5 - Power Supply Requirements (After Programming)

Supply Name

Supply Name