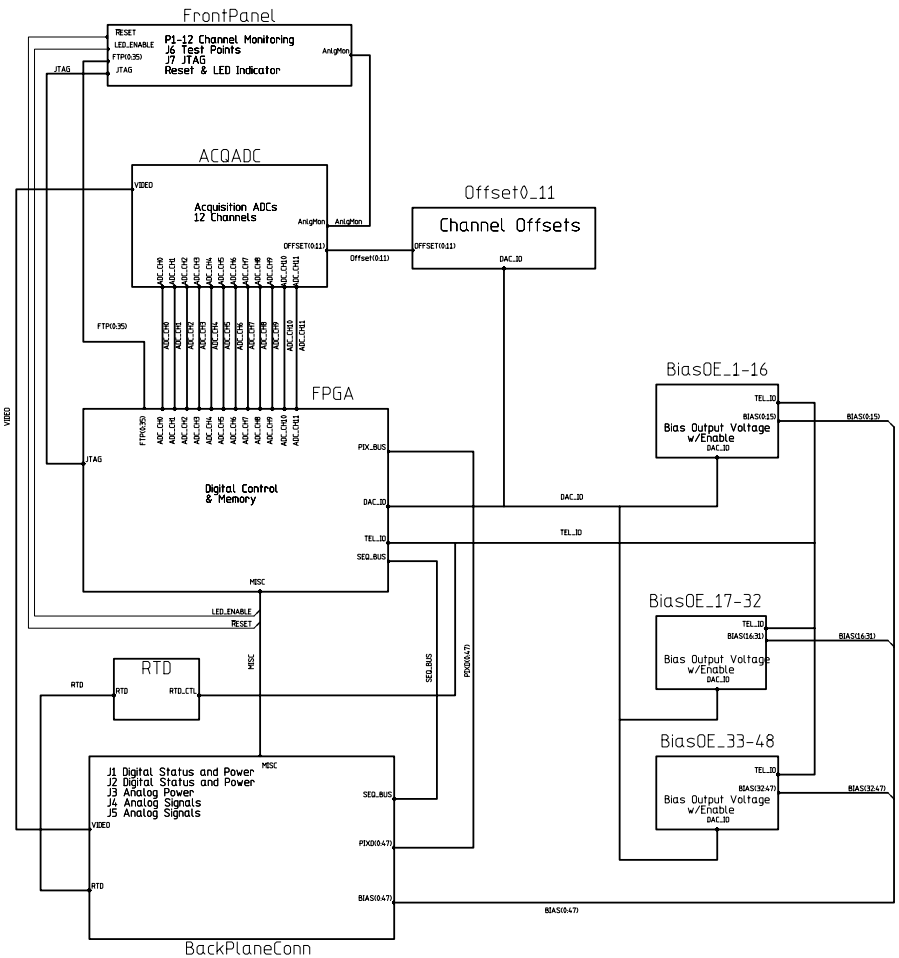
Remove inductors from input power.
Change the fuse rating
Add a wire to temperature sensor chip-select (pin 3) so it connects to FPGA pin AD20. As a temperary fix we connected pin 3 to pin 6.
Change R180 to 0 Ohms.
Found the Inv and NonInv lines swapped on Channels 5 & 7 (counting from 0). The error is on the schematic therefore the PCB too.
Change resistor divider from ADCREF 9.09K|11K to 2K|8K..
R39,R84,R123,R166,R696,R741,R780,R823,R863,R906 -> 11K
R33,R78,R117,R160,R690,R735,R774,R817,R862,R901 -> 8K
Change the resistors on Telemetry ADCs..
RefDes ADC Input Resistor
R247,R446,R257,R407,R408,R409,R410,R411,R412,R413,R263,R369,R370,R371,R372,R373,R374,R375 ->6.8K
R447,R448,R449,R450,R451,R467,R2,R927,R9,R926,R10,R925,R11,R928,R268,R324,R325,R326,R327,R328,R329,R330 ->0
R275,R278,R279,R280,R281,R282,R283,R284 ->20K
Add the following wires:

NetName	End-End	FPGA pin
PIXD(27)	TPF08 to RN30-16	C27
AD1_SYNC	TPF04 to via at C278	G25

Make sure R270 & R317 are not installed
Change U91 from DS2401 to DS2433 SO8 package.
Front panel test jacks need to be different type. The Dual Lemos do not fit! Recommend using minature coax plug.
Rotate the three LEDs D8,9,10 180°



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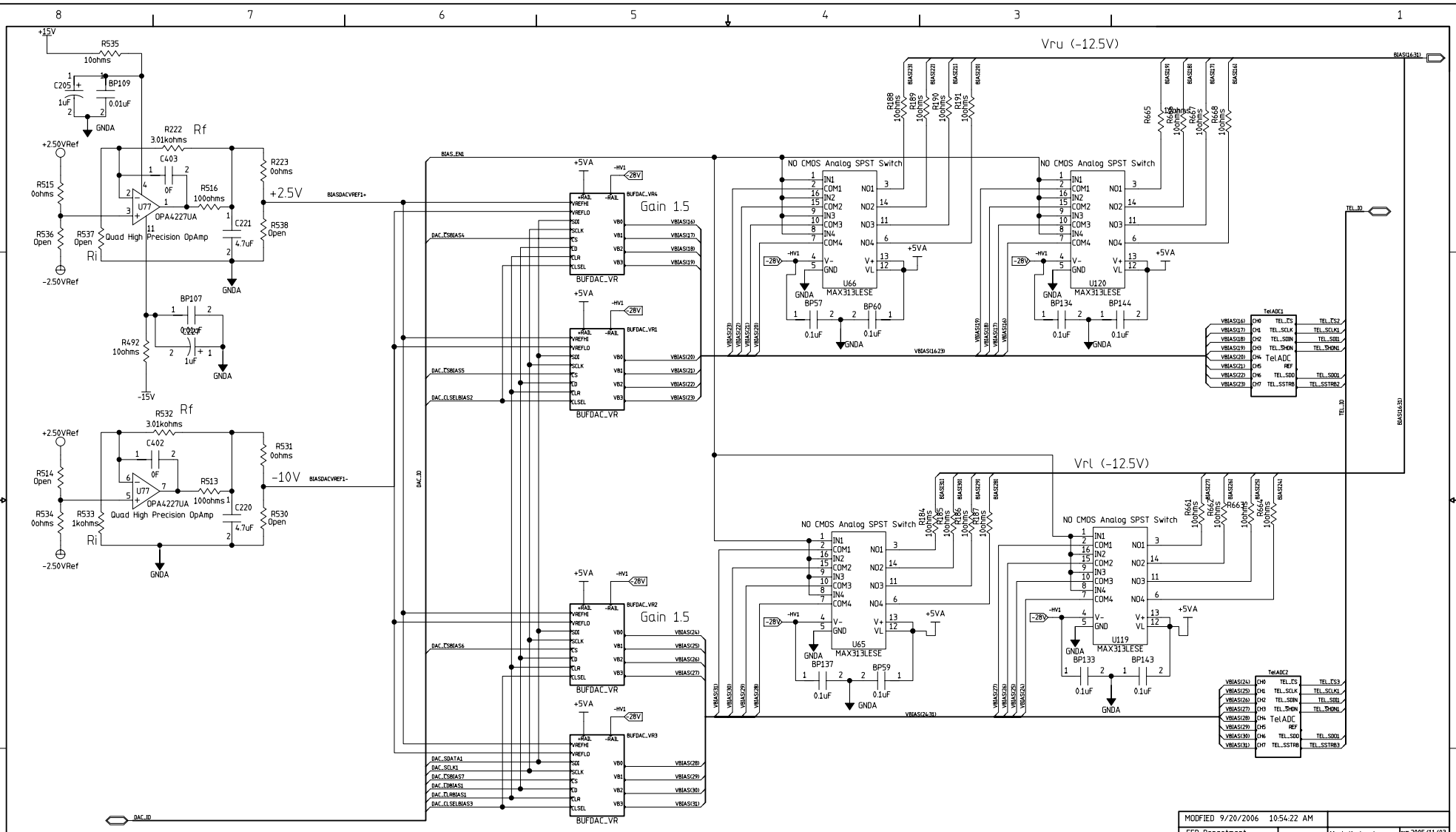
ACQUISITION BOARD TOP LEVEL

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H:BND: V:4LA



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Bias Output w/Enable 17-32

SIZE	DRAWING NUMBER		REV
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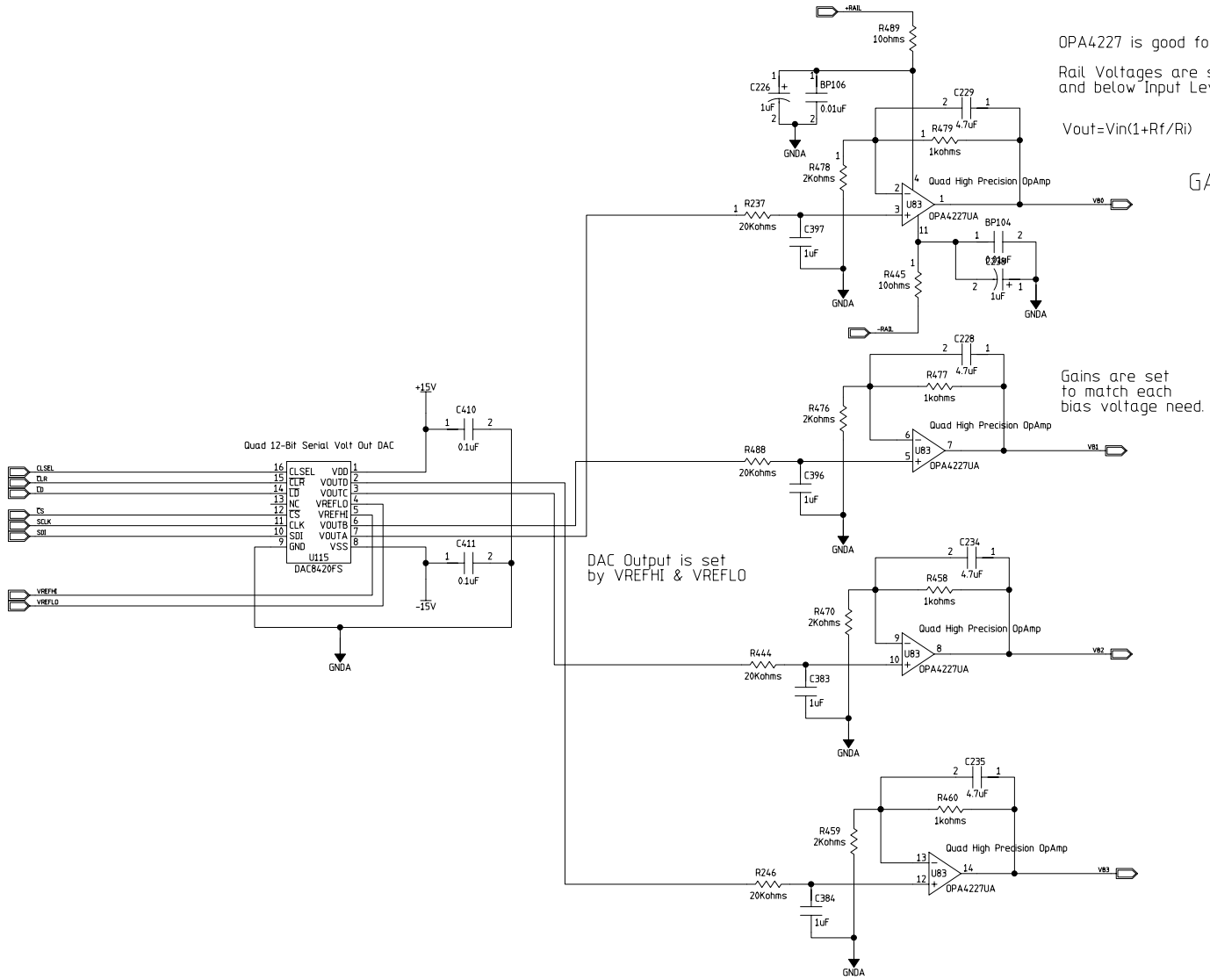
H:BND: V:4LA


+RAIL
R489
10ohms
C226
1uF
BP106
0.01uF
GNDA
C229
4.7uF
R479
1kohms
R478
2Kohms
Quad High Precision OpAmp
U83
OPA4227UA
VB0
R237
20Kohms
C397
1uF
BP104
R445
10ohms
-RAIL
C228
4.7uF
R477
1kohms
R476
2Kohms
Quad High Precision OpAmp
U83
OPA4227UA
VB1
R488
20Kohms
C396
1uF
C234
4.7uF
R458
1kohms
R470
2Kohms
Quad High Precision OpAmp
U83
OPA4227UA
VB2
R444
20Kohms
C383
1uF
C235
4.7uF
R460
1kohms
R459
2Kohms
Quad High Precision OpAmp
U83
OPA4227UA
VB3
R246
20Kohms
C384
1uF
+15V
C410
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
CLSEL VDD
CLR VOUTD
LD VOUTC
NC VREFLO
CS VREFHI
CLK VOUTB
SDI VOUTA
GND VSS
U115
DAC8420FS
C411
0.1uF
-15V
DAC Output is set
by VREFHI & VREFLO
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
Gains are set
to match each
bias voltage need.
Vr BIAS CHANNELS 16-19
MODIFIED 10/25/2006 10:22:48 AM
EED Department
Page 10 -2
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
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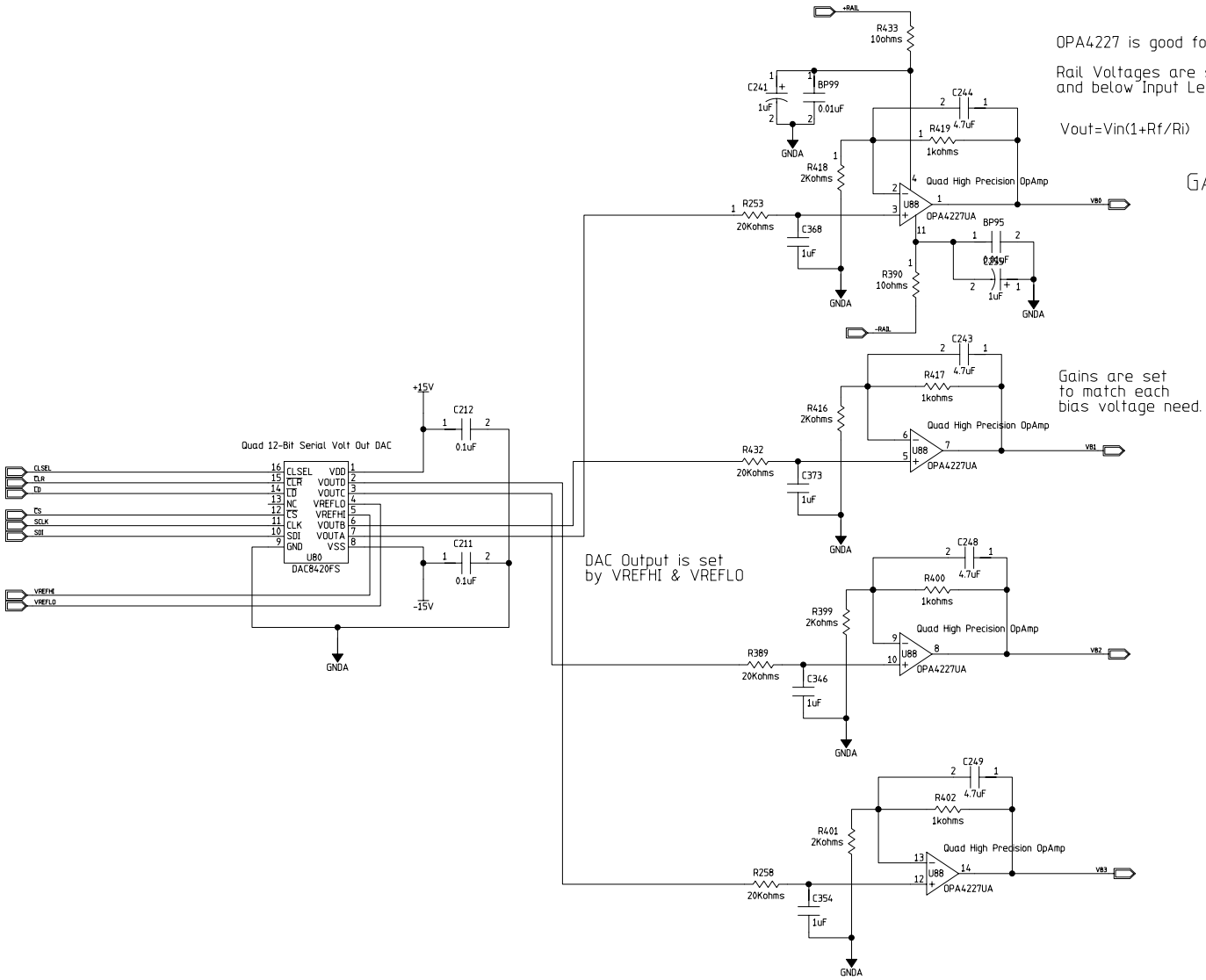
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.5

Gains are set
to match each
bias voltage need.

Vr BIAS CHANNELS 28-31

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4 Channel Buffer DAC - VR

SIZE	DRAWING NUMBER		REV
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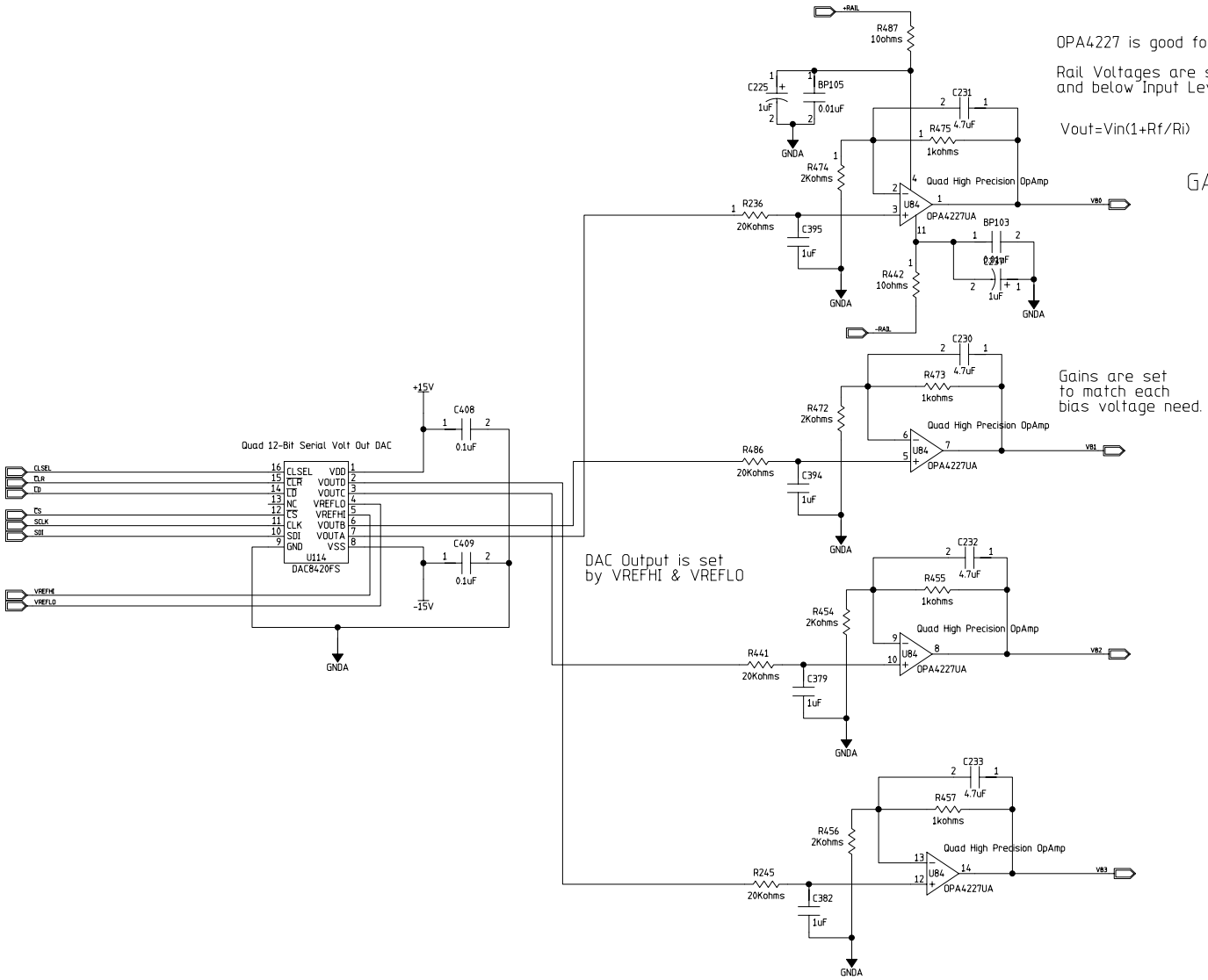
H:BND: V:4LA



Vr BIAS CHANNELS 24-27

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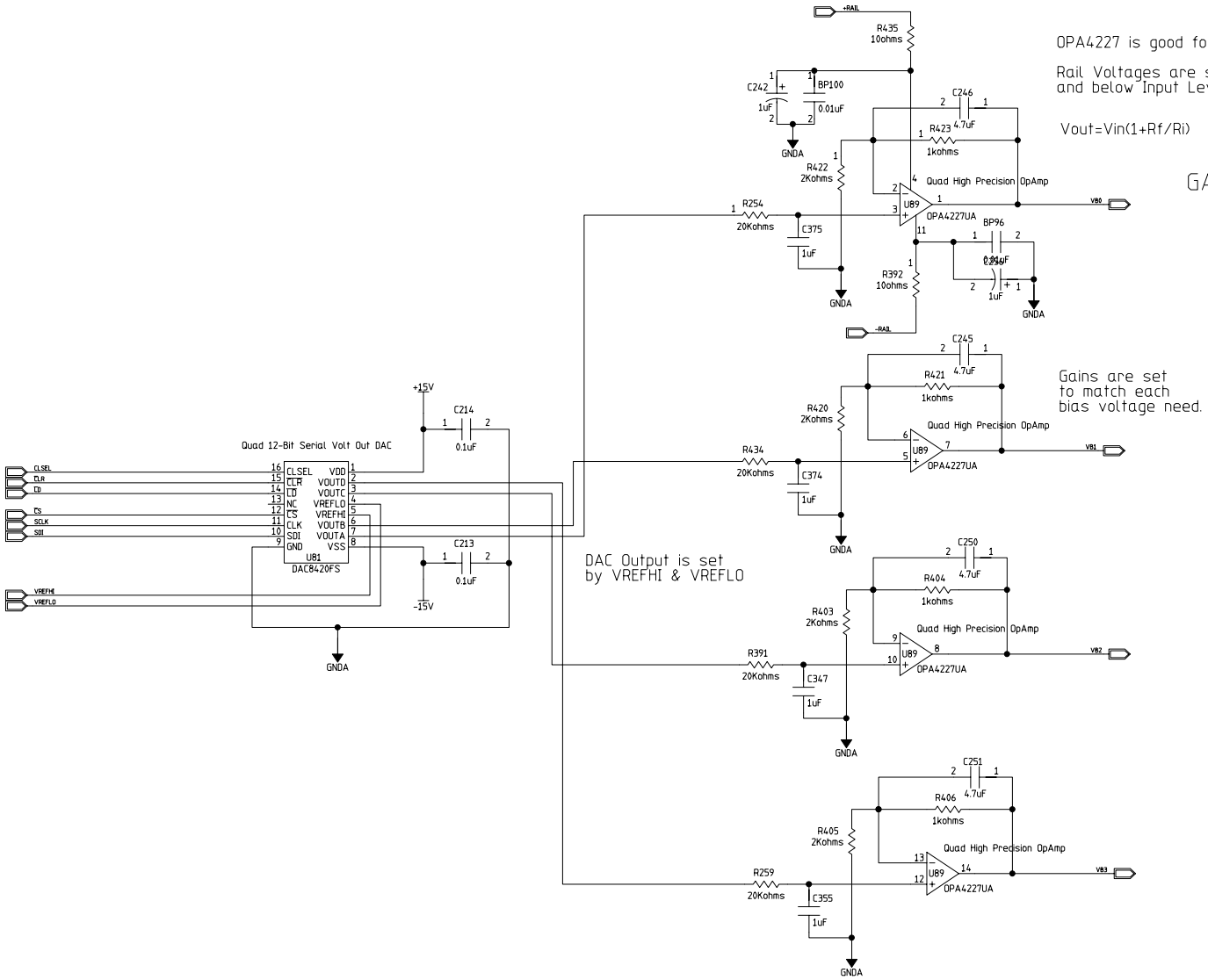
4 Channel Buffer DAC - VR

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.5

Gains are set
to match each
bias voltage need.

Vr BIAS CHANNELS 20-23

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4 Channel Buffer DAC - VR

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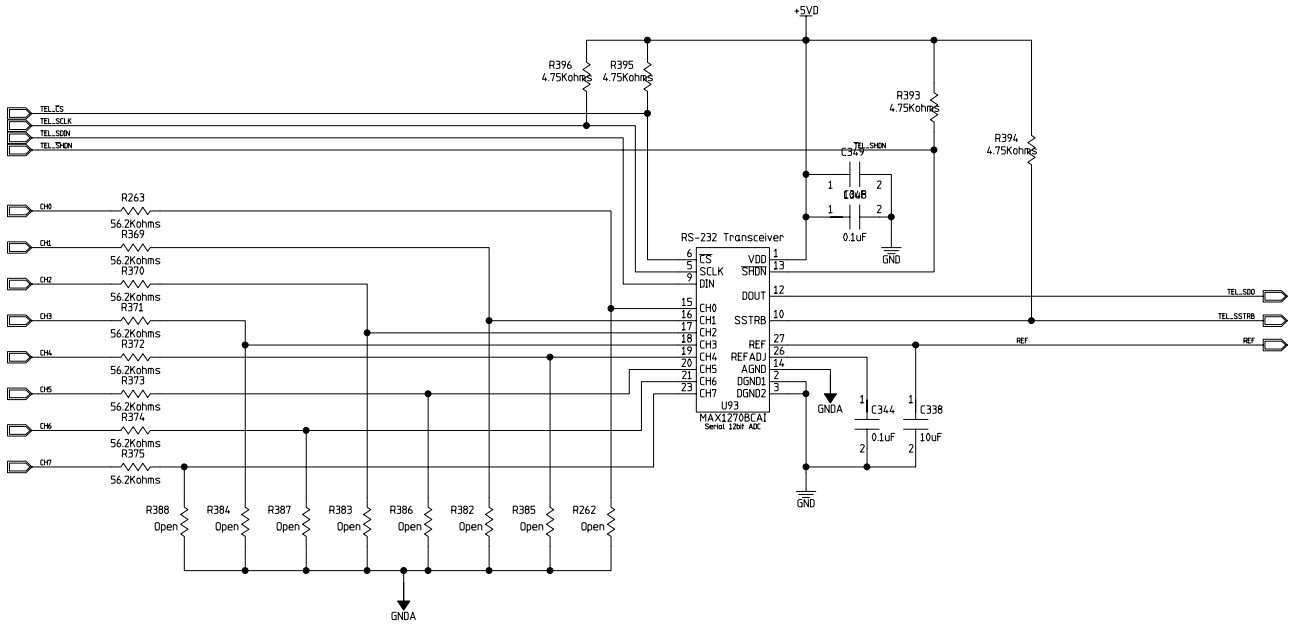
H:BND: V:4LA



TELEMETRY CHANNELS BIAS 24-31

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8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
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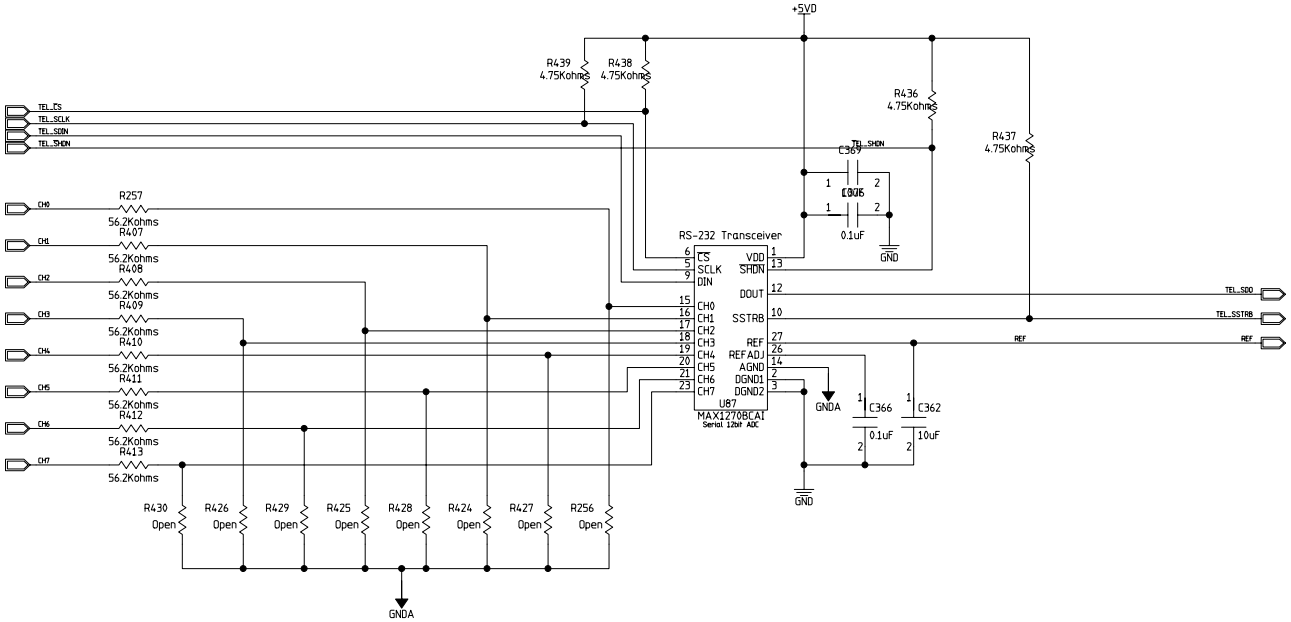

TELEMETRY CHANNELS BIAS 16-23

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8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
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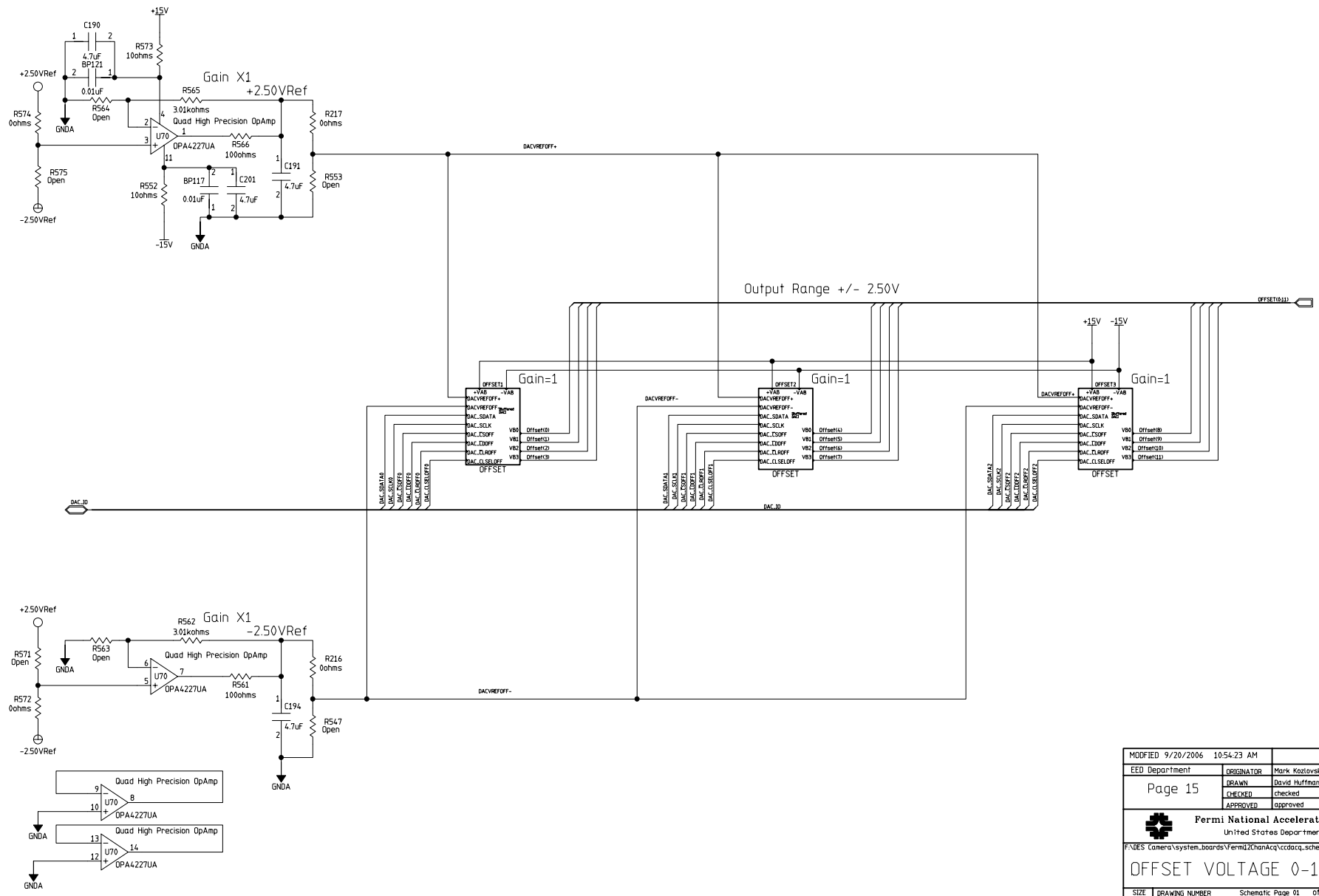

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OFFSET VOLTAGE 0-11

SIZE	DRAWING NUMBER		REV
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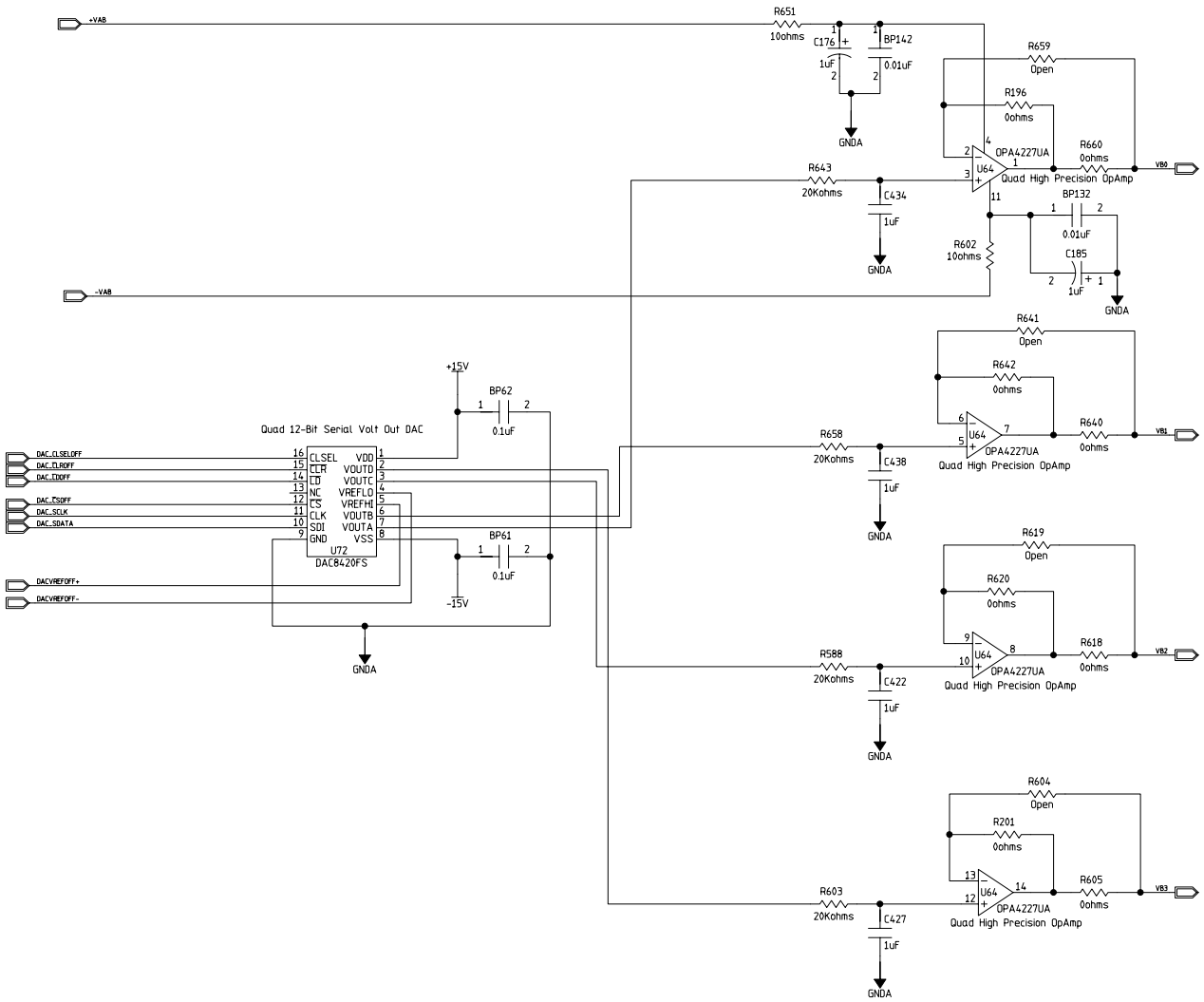
H:BND: V=4LA



OFFSET DAC CHANNELS 0-3

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OFFSET DAC

SIZE	DRAWING NUMBER		REV
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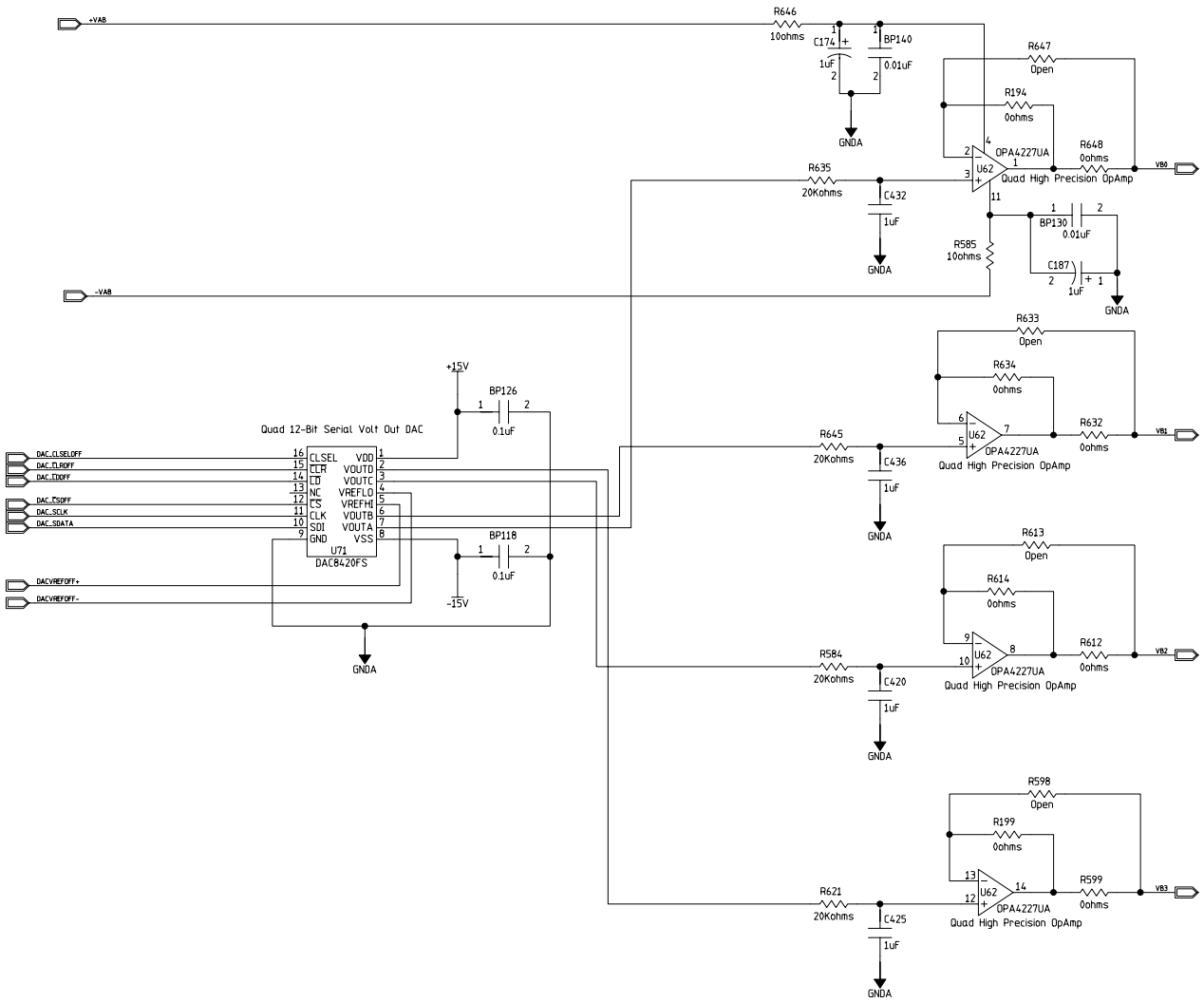

OFFSET DAC CHANNELS 8-11

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OFFSET DAC

SIZE	DRAWING NUMBER		REV
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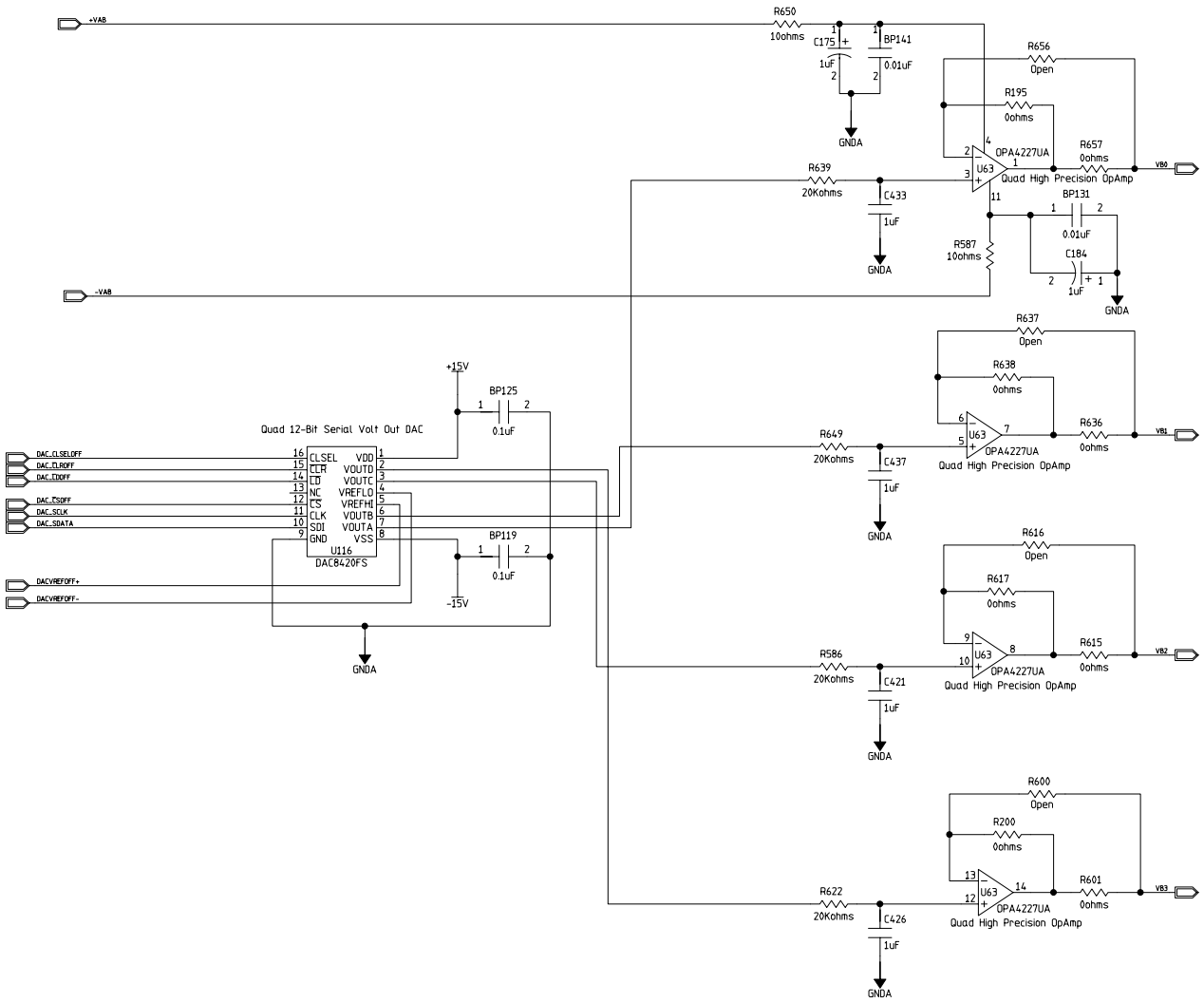

OFFSET DAC CHANNELS 4-7

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OFFSET DAC

SIZE	DRAWING NUMBER		REV
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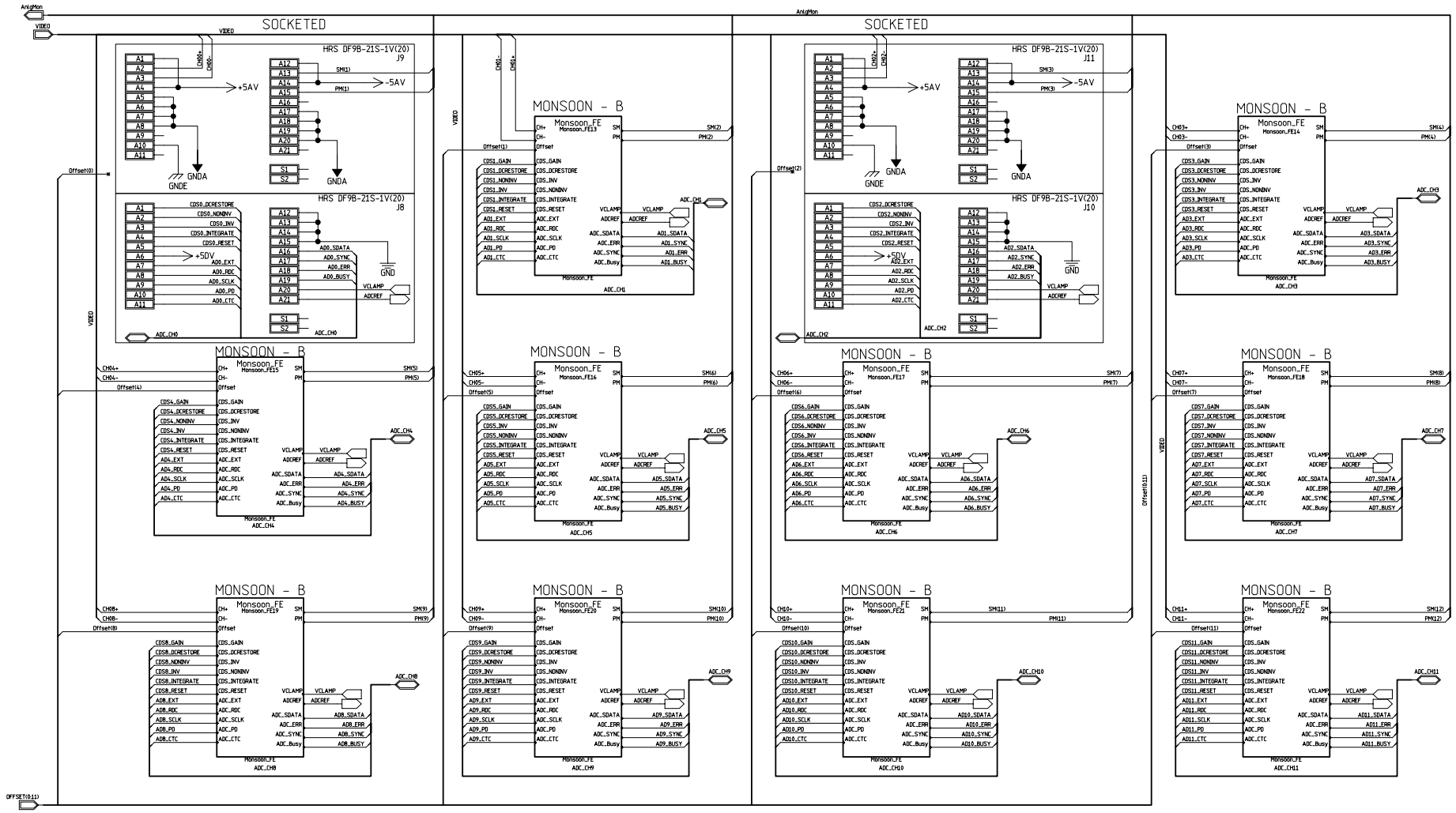

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ACQUISITION ADCs

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
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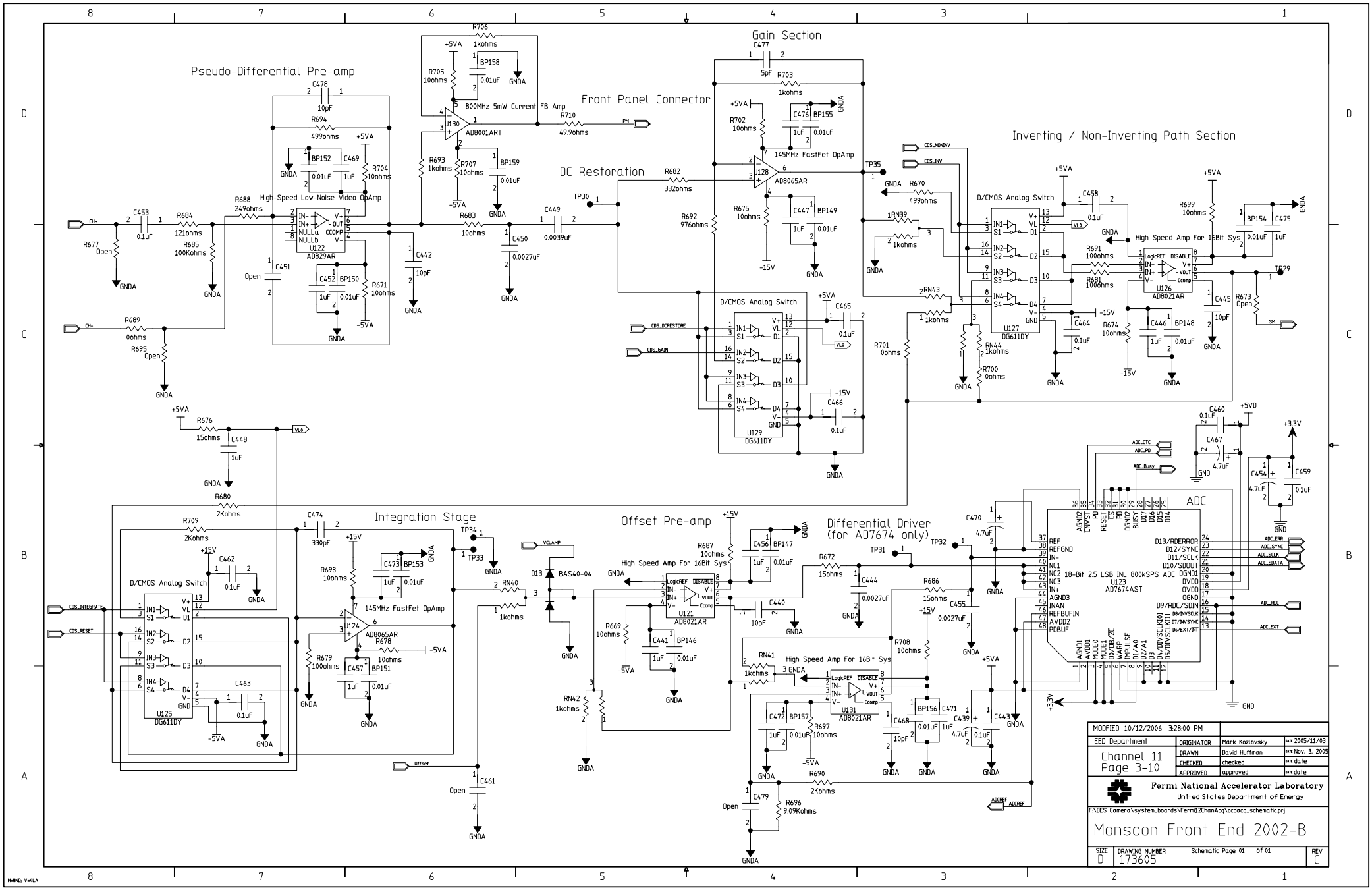
Pseudo-Differential Pre-amp
Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
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EED Department
Channel 11
Page 3-10
ORIGINATOR Mark Kozlovsky 2005/11/03
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APPROVED approved date
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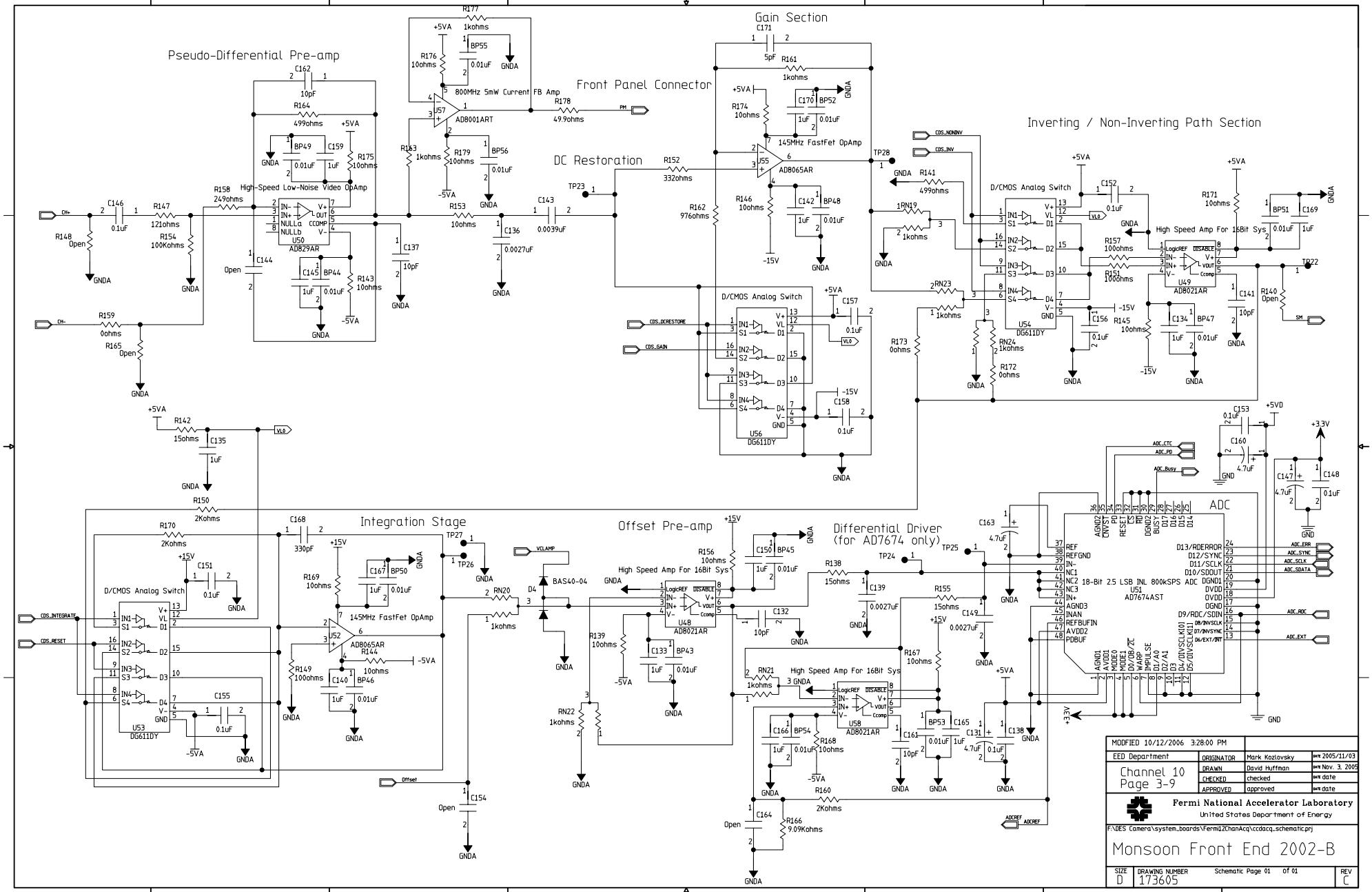
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C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Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
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ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
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18-Bit 2.5 LSB INL 800kSPS ADC
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Channel 10
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SIZE D
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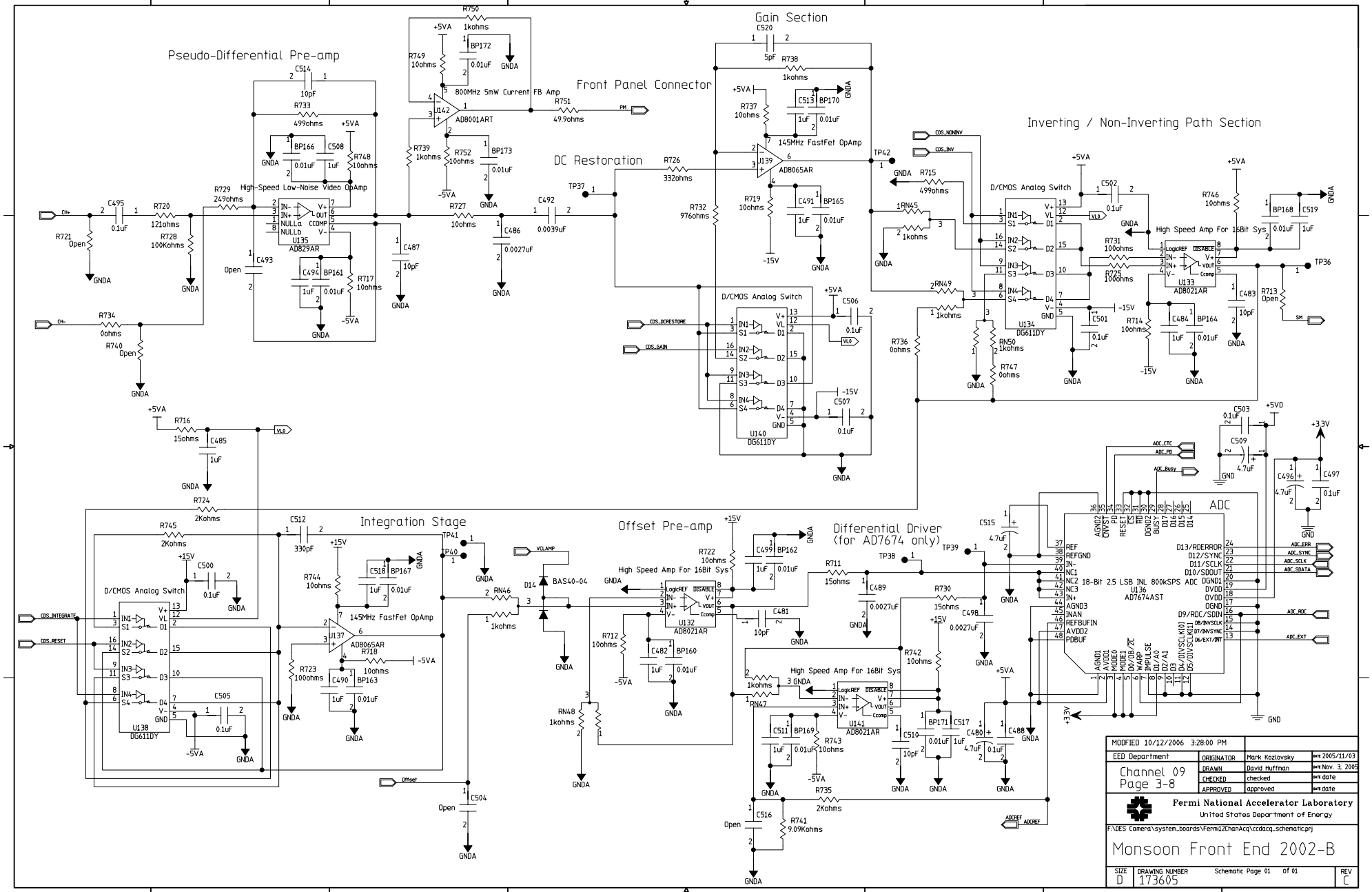
REV C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DC Restoration
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High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
High Speed Amp For 16Bit Sys
D/CMOS Analog Switch
18-Bit 2.5 LSB INL 800kSPS ADC
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EED Department
Channel 09
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DRAWING NUMBER 173605
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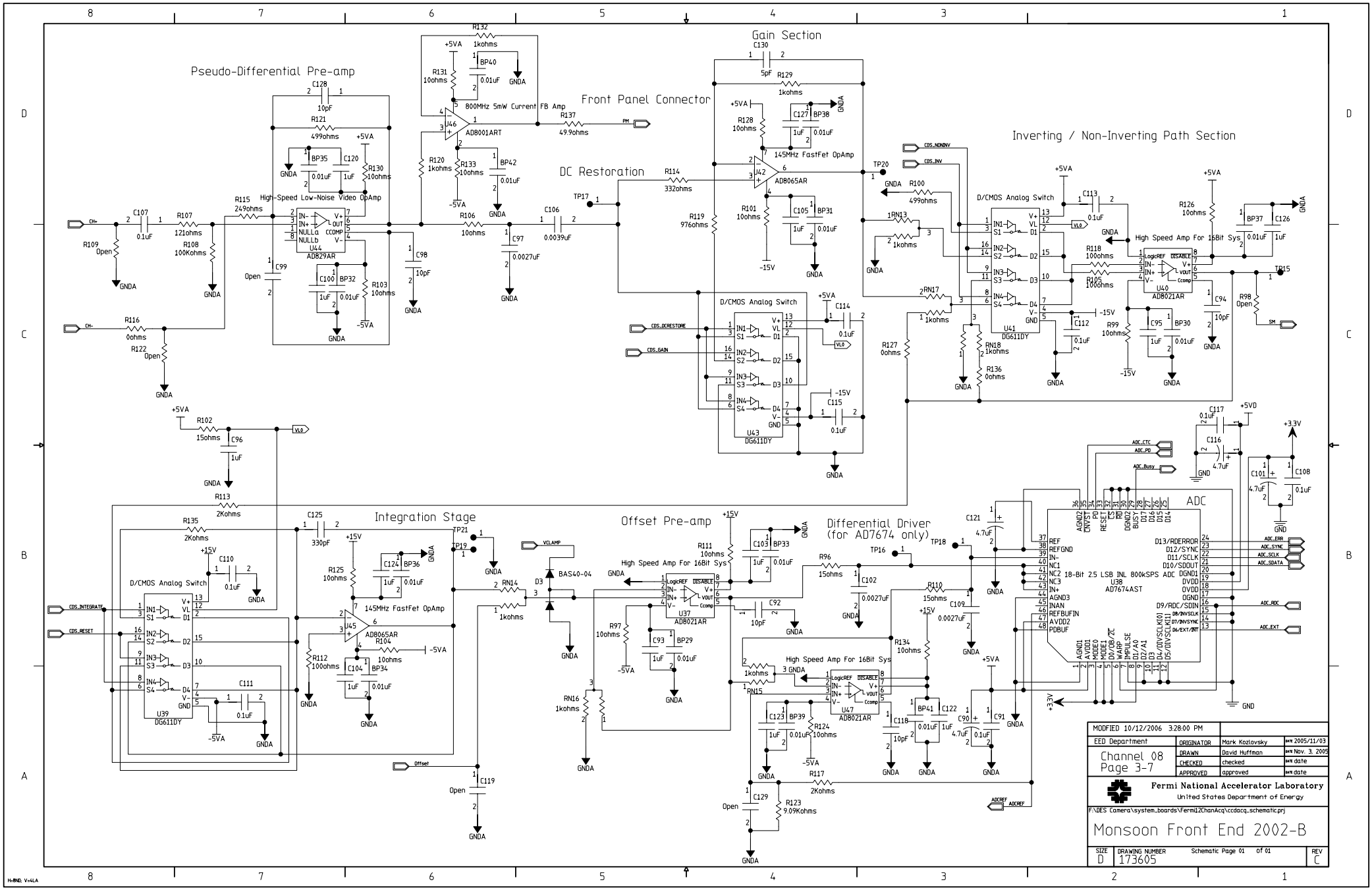
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Gain Section
Front Panel Connector
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ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
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Channel 08
Page 3-7
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SIZE D
DRAWING NUMBER 173605
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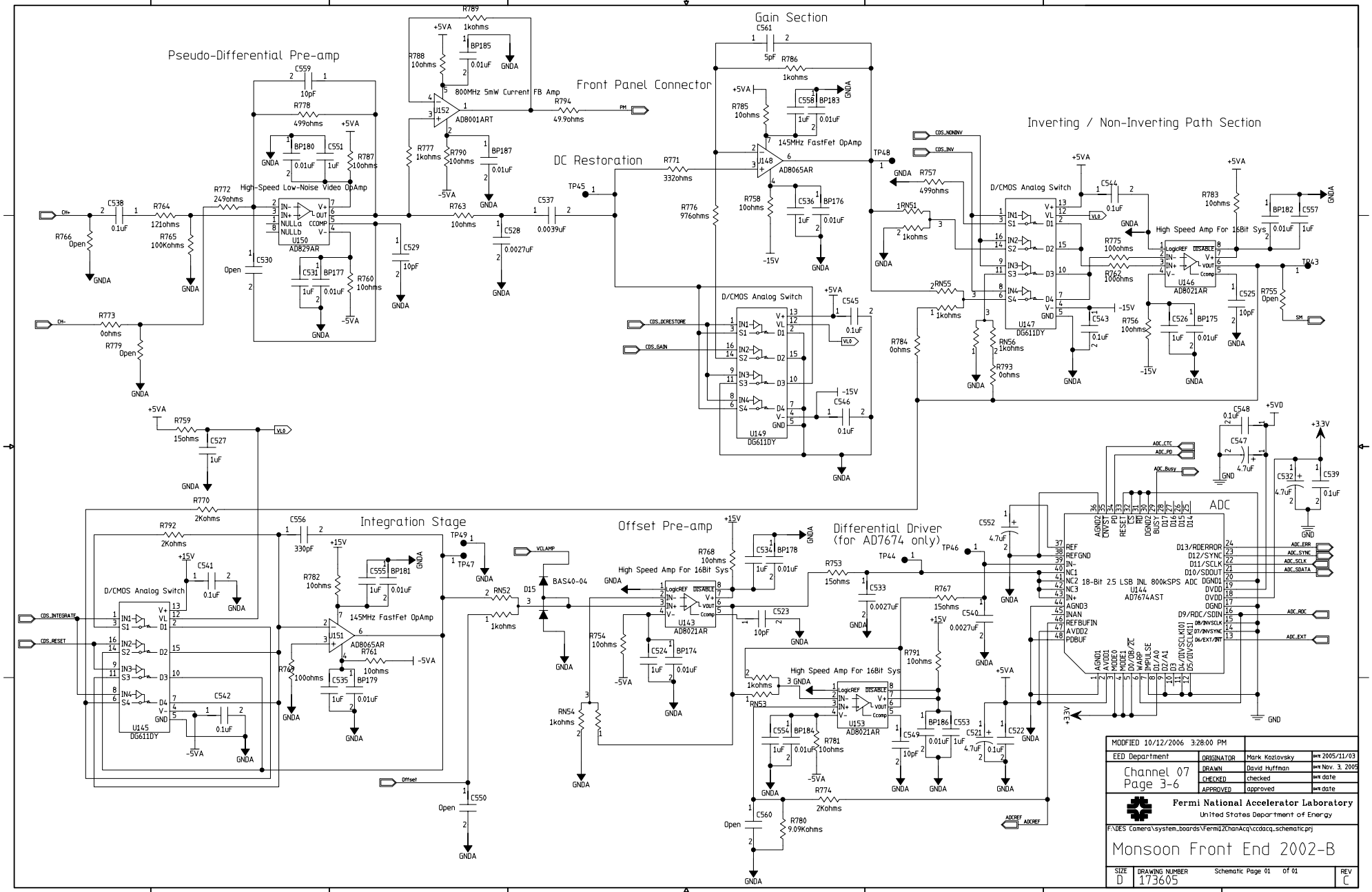
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Inverting / Non-Inverting Path Section
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High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
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Channel 07
Page 3-6
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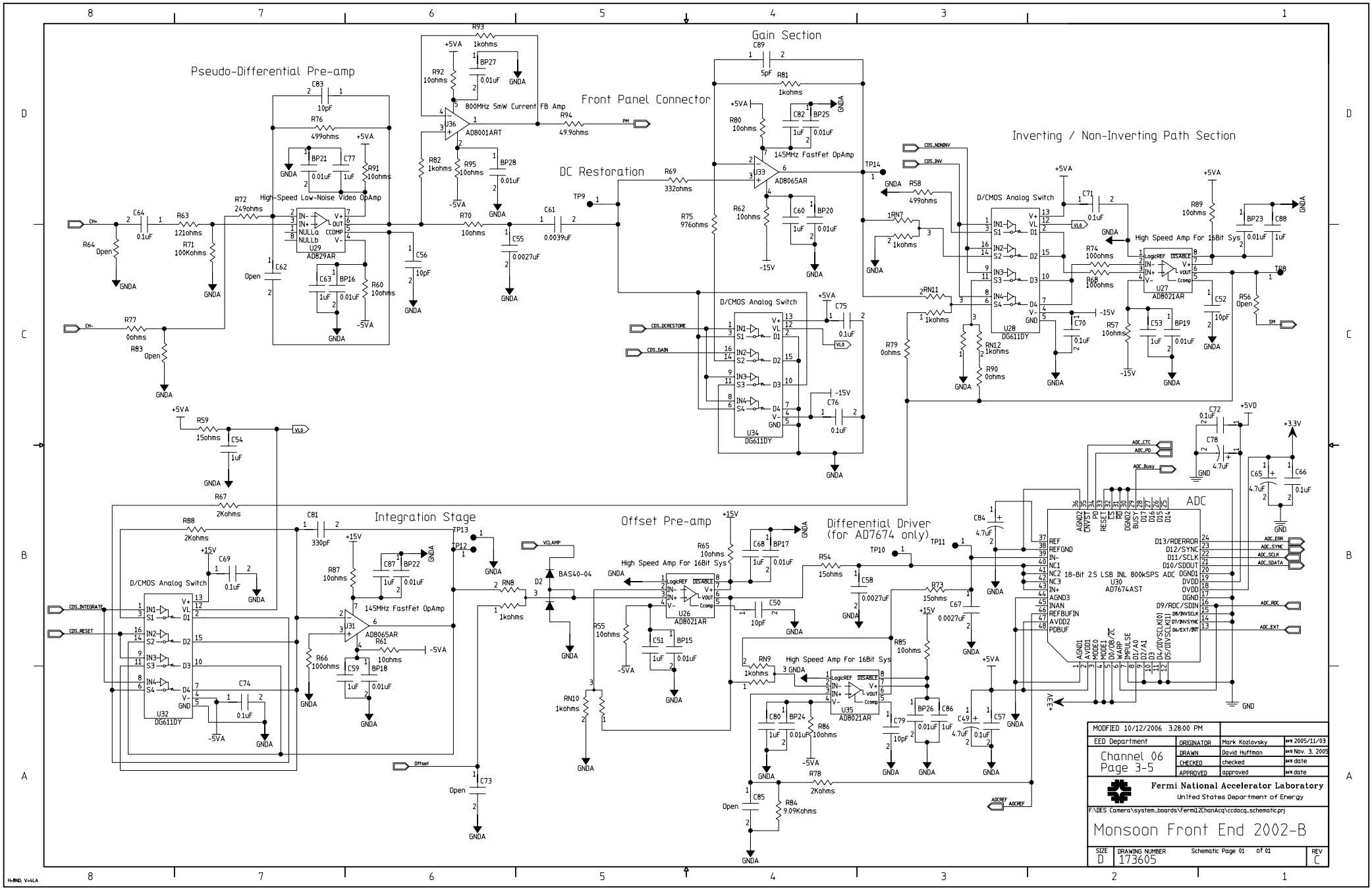
REV C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Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
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Channel 06
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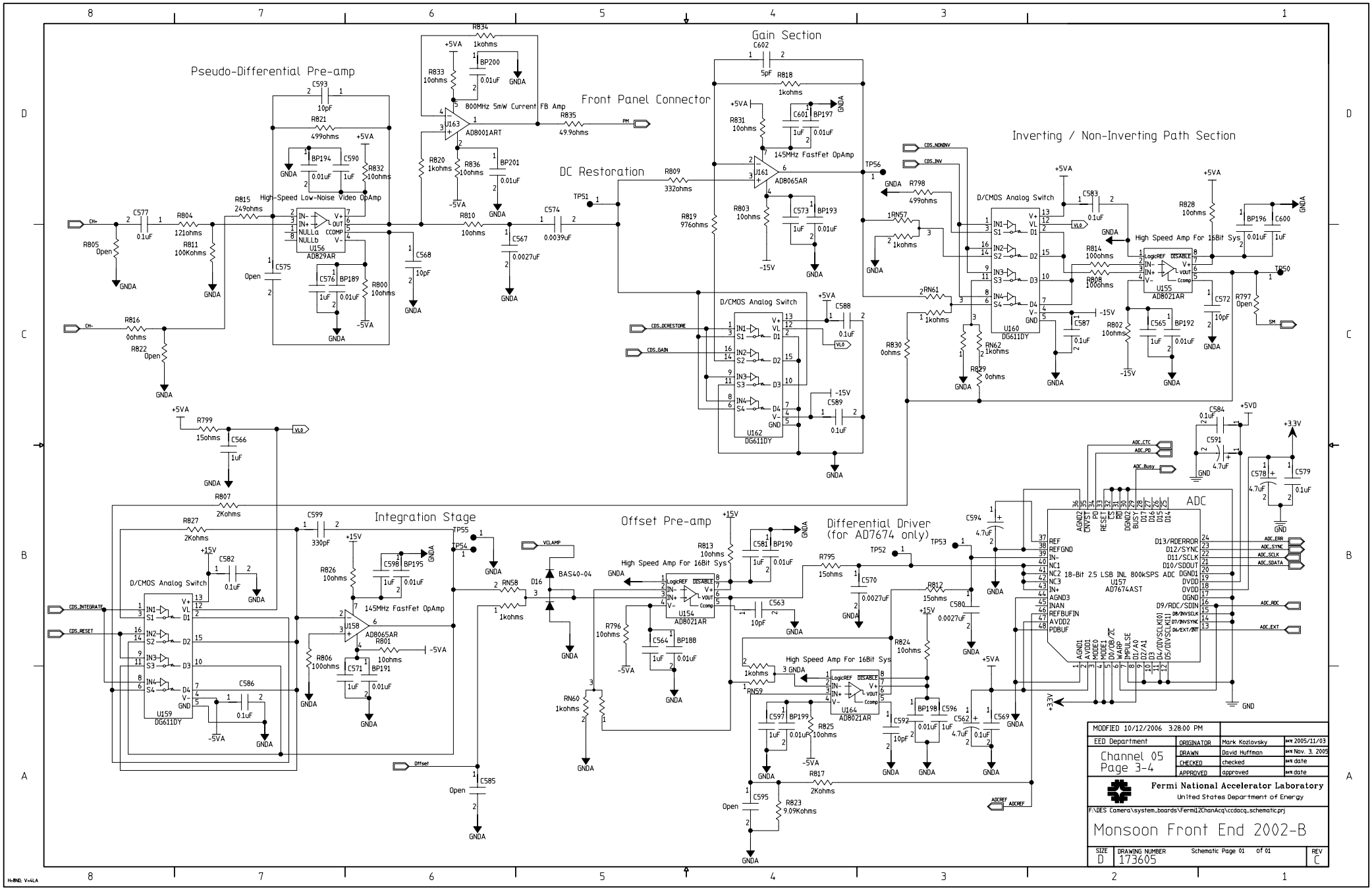
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Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
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Schematic Page 01 of 01
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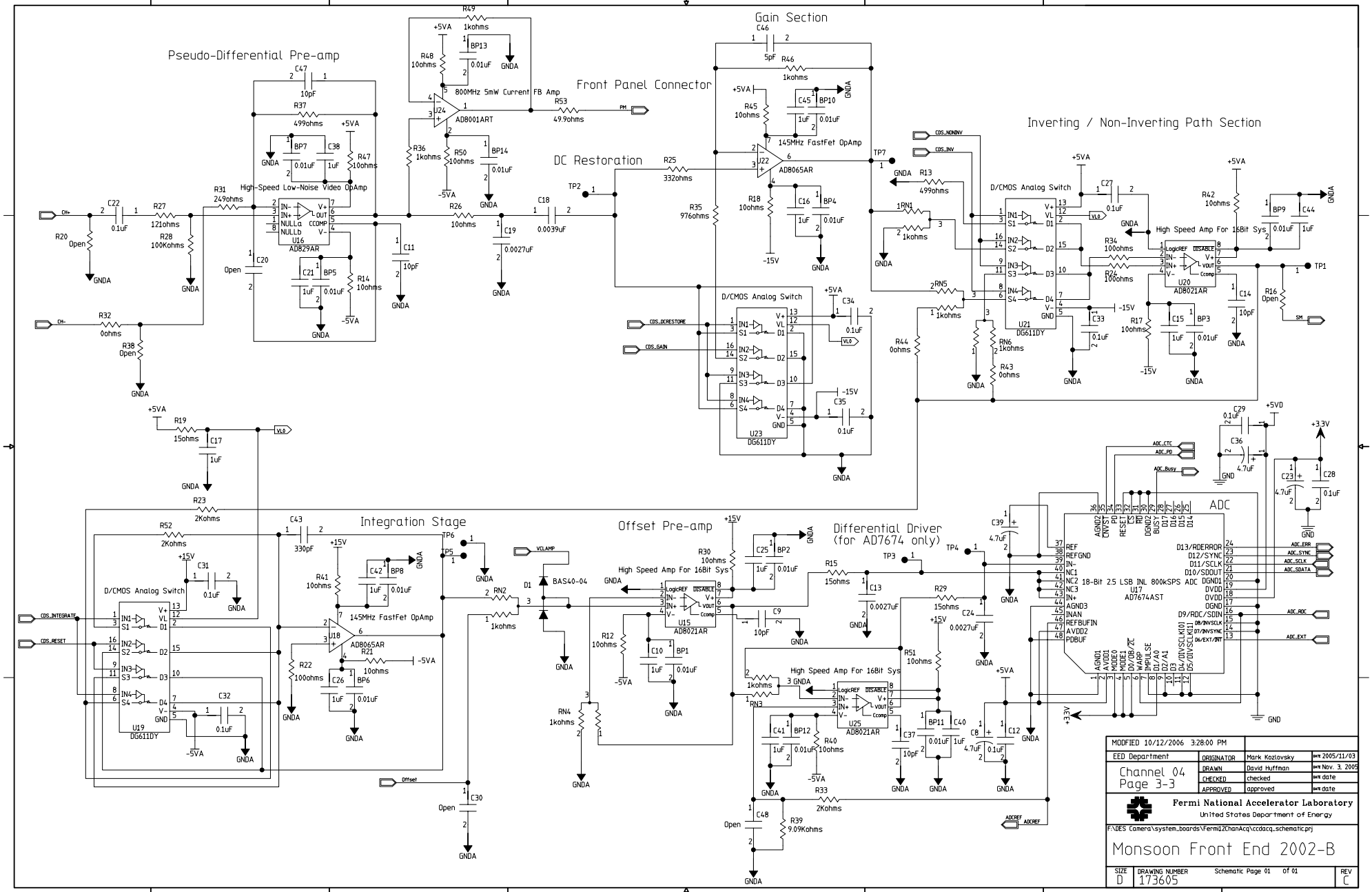
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Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
High Speed Amp For 16Bit Sys
D/CMOS Analog Switch
18-Bit 2.5 LSB INL 800kSPS ADC
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Channel 04
Page 3-3
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
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Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
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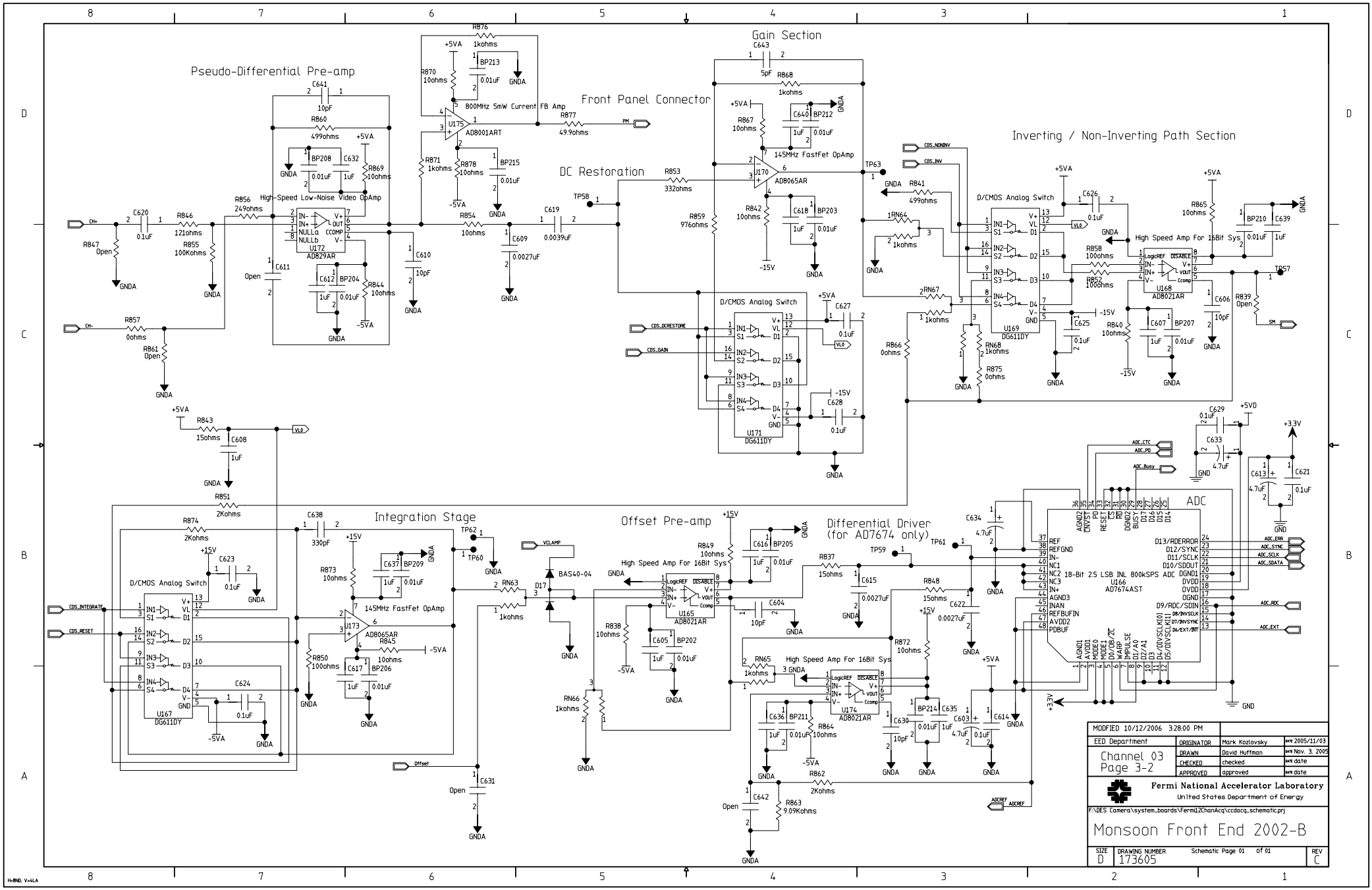
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DRAWN David Huffman Nov. 3, 2005
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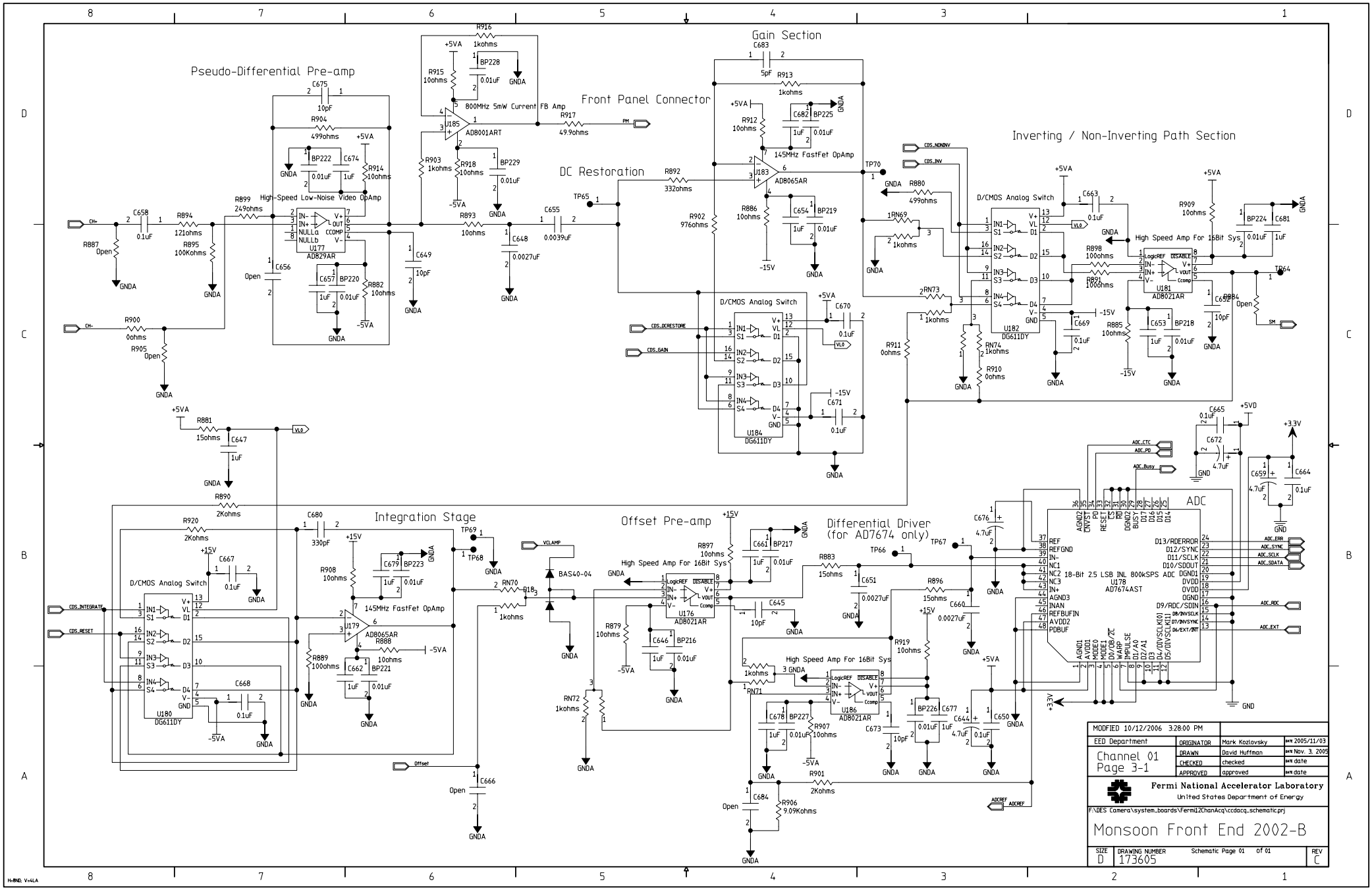
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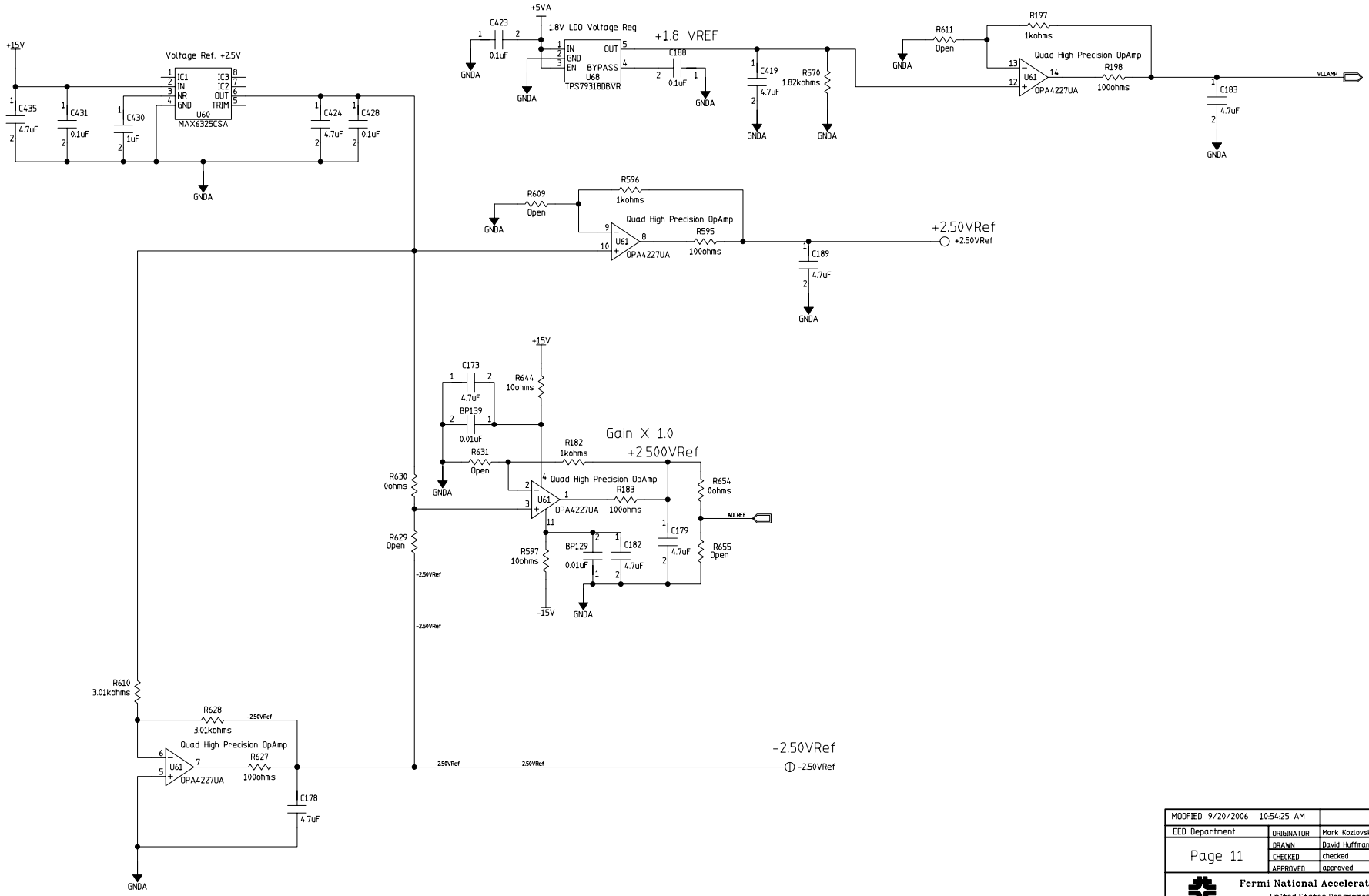

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ADC REFERENCE and CLAMP Voltages

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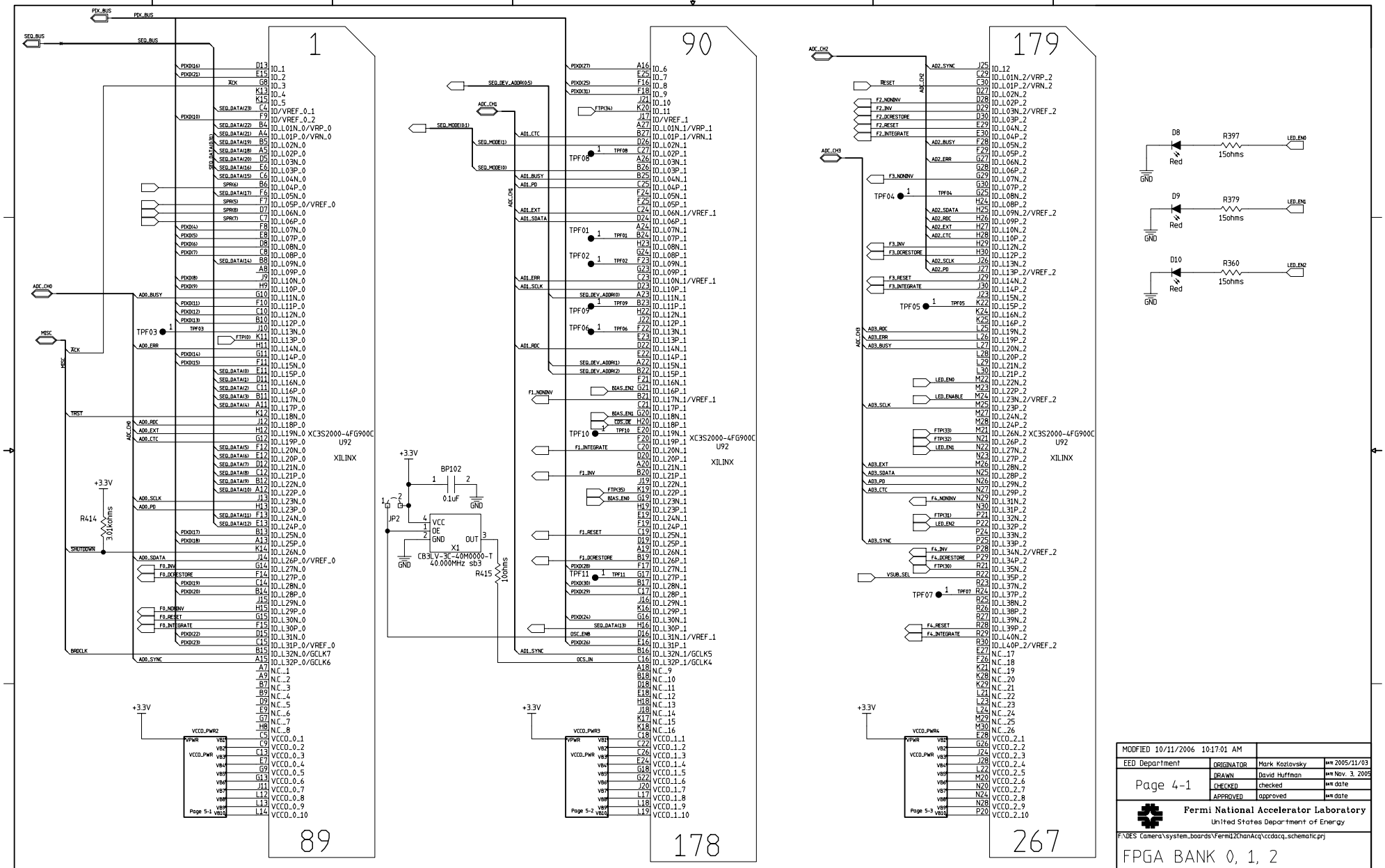

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FPGA BANK 0, 1, 2

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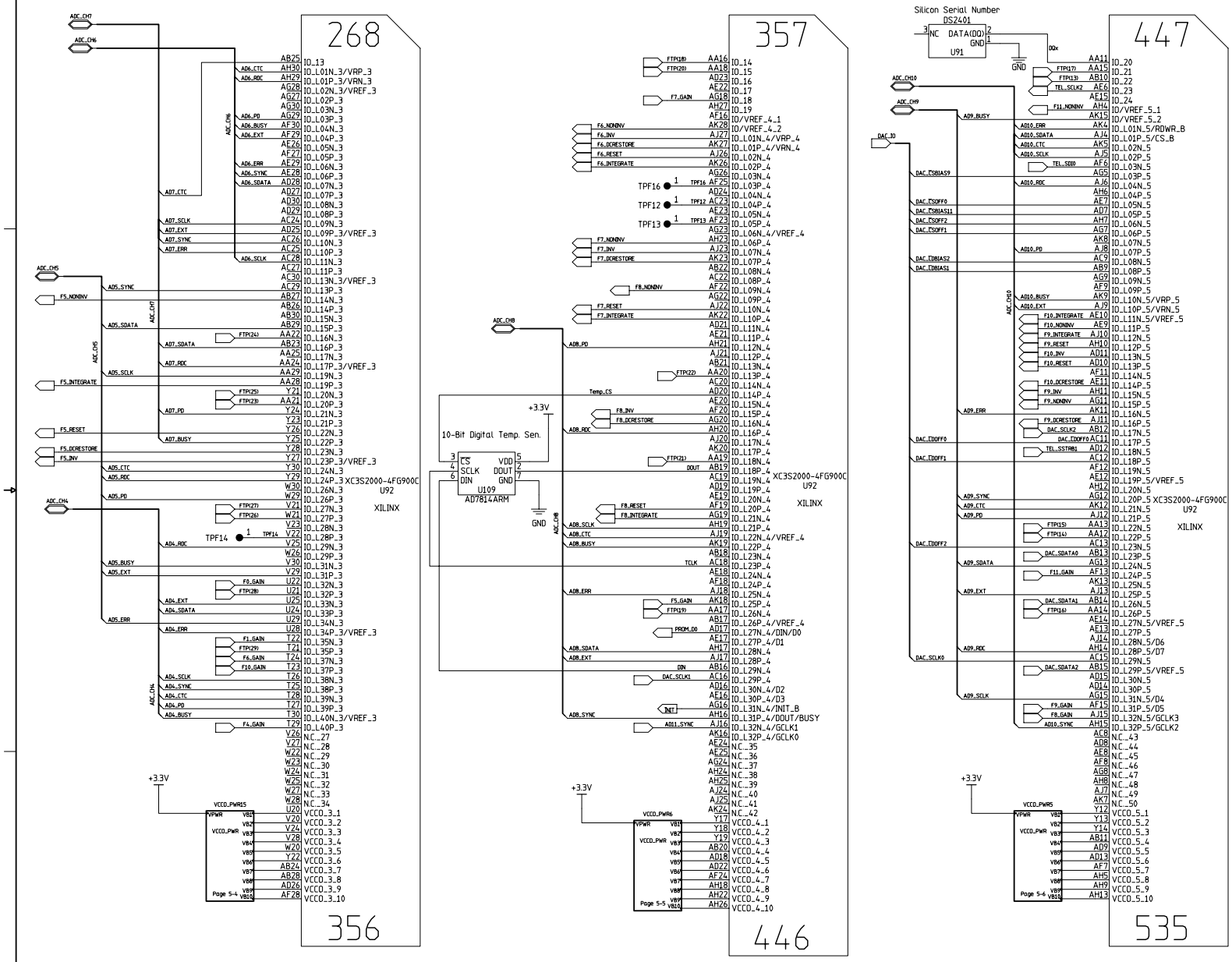

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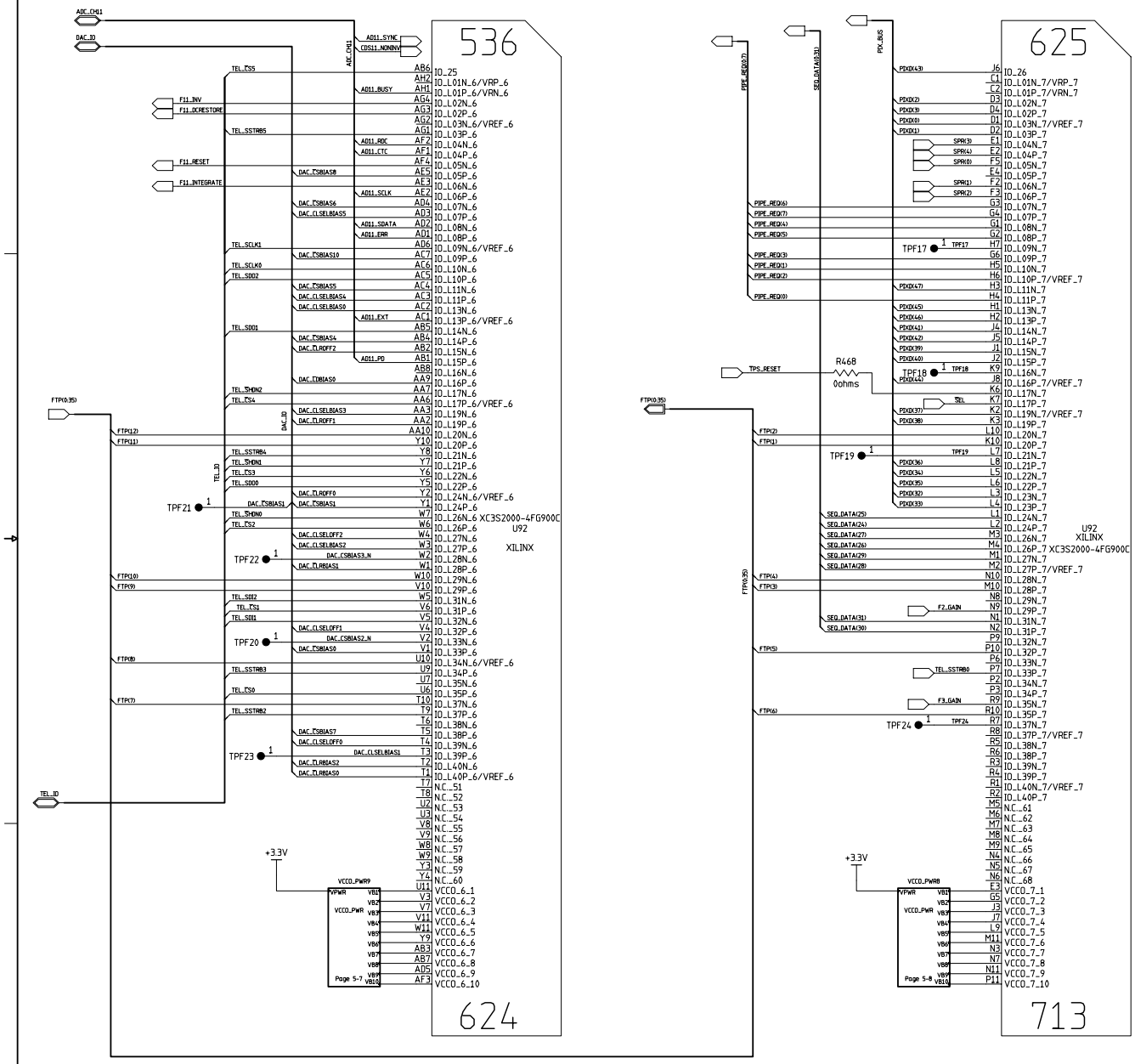

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FPGA BANK 6, 7

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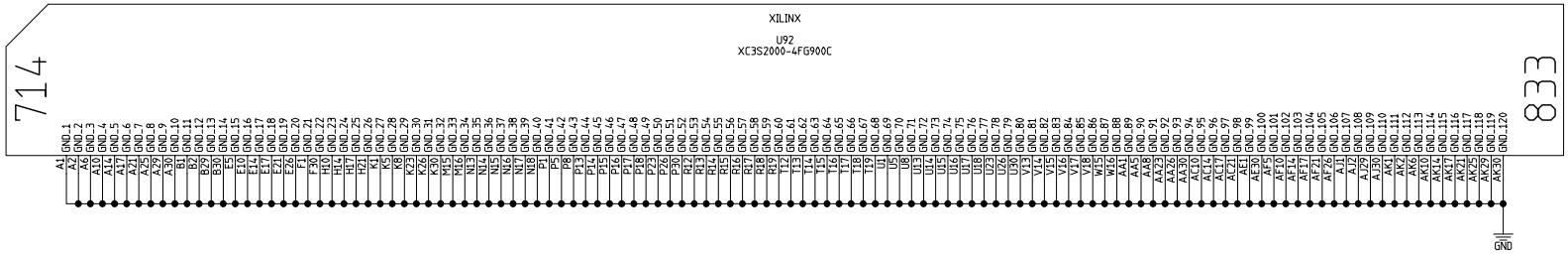

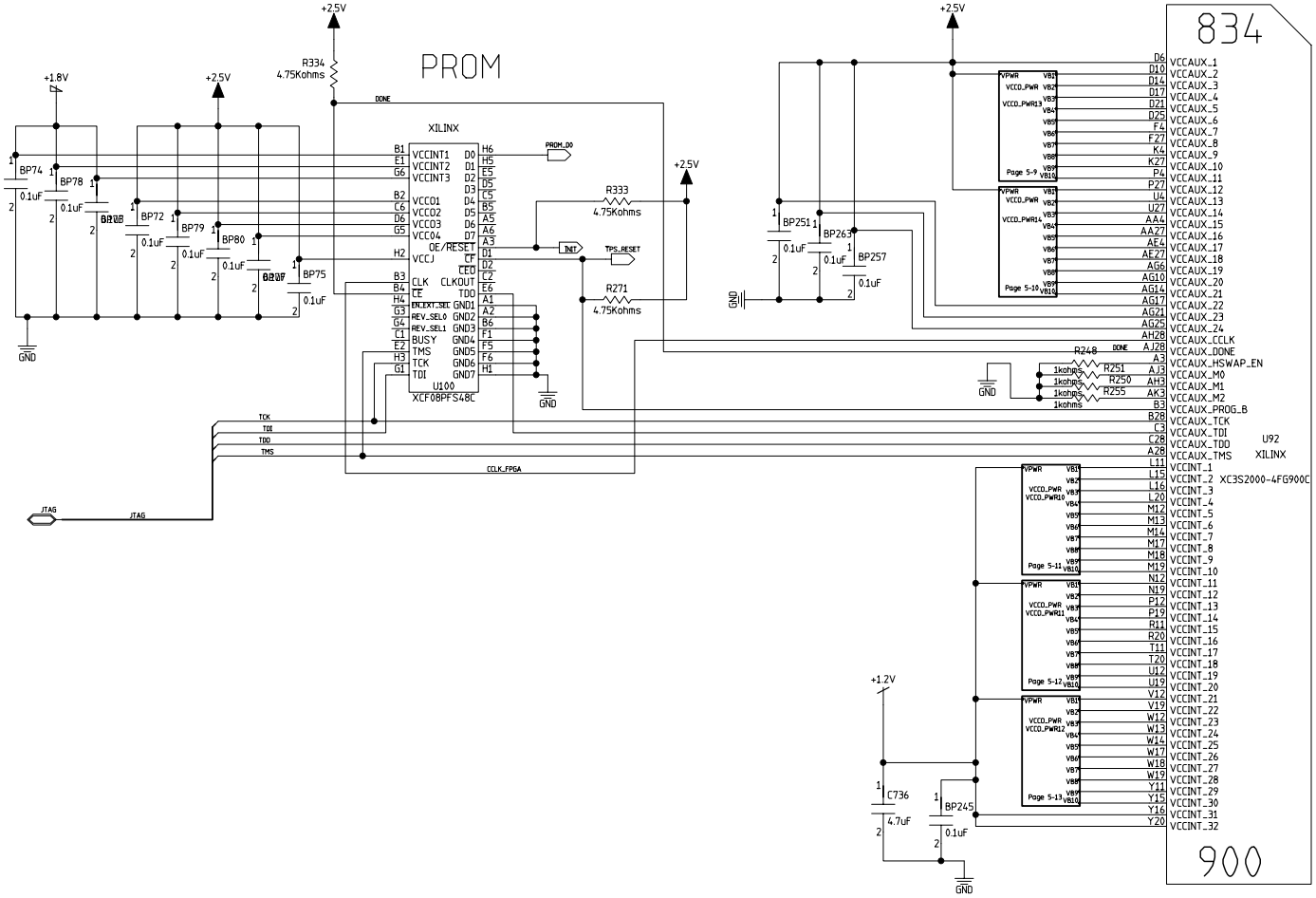

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PROM Power & Ground

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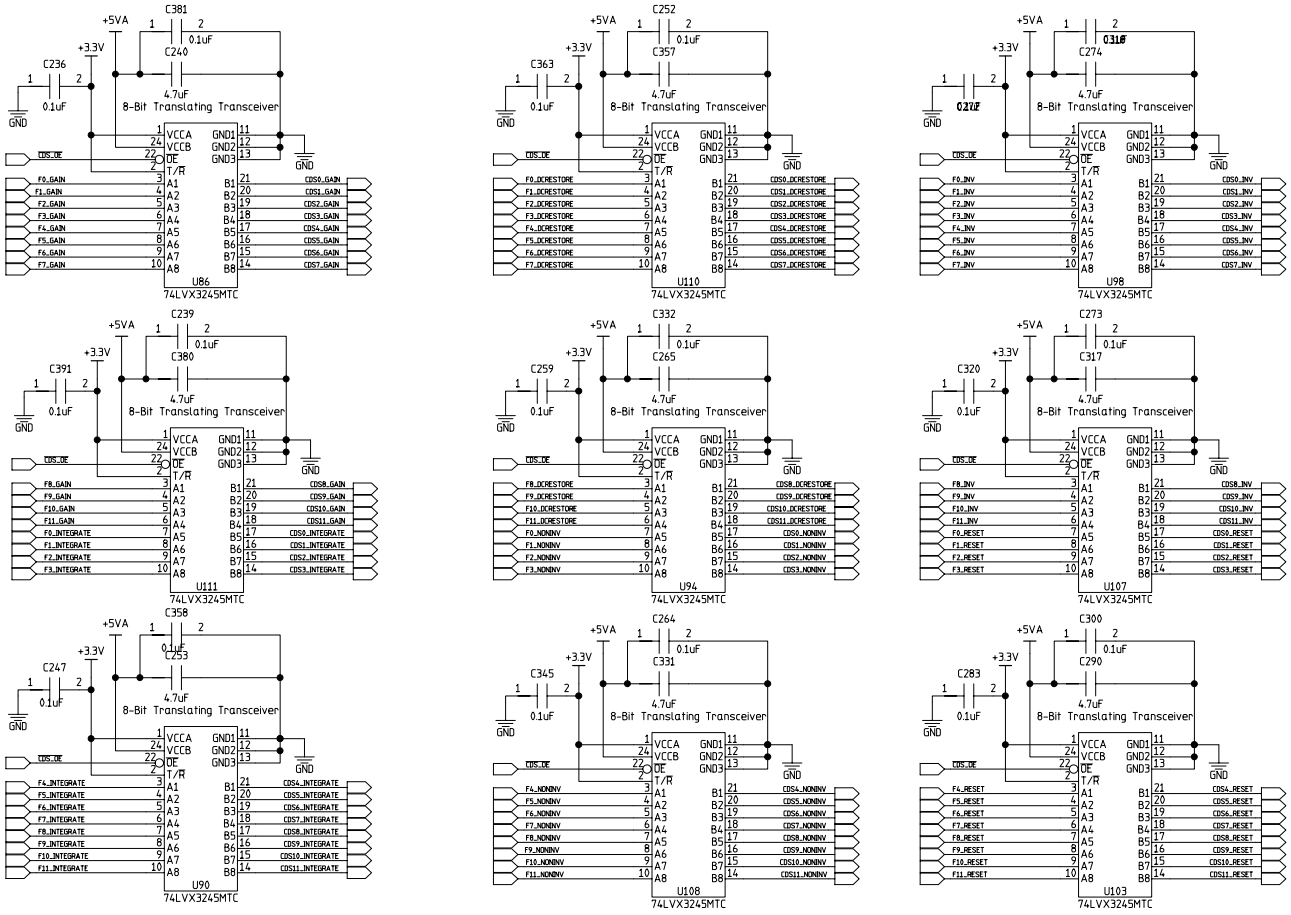

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Level Translators

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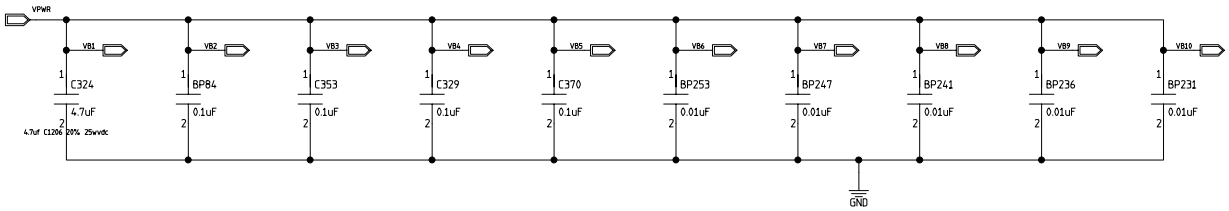

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Power Rail By-Passing

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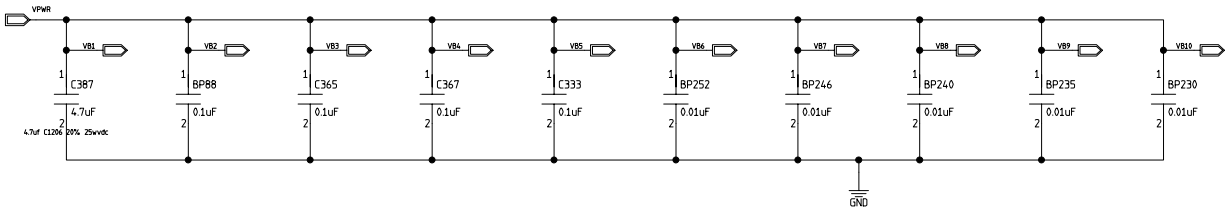

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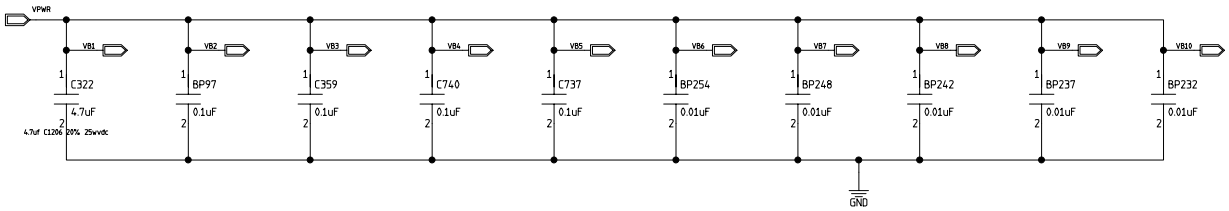

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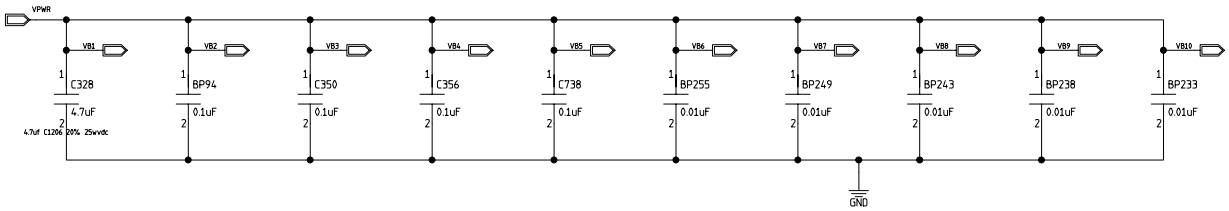

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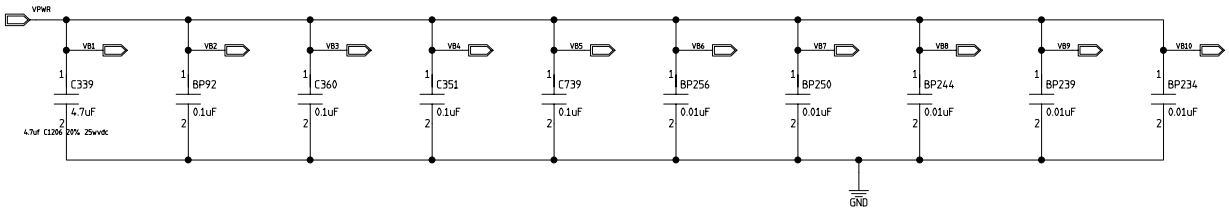

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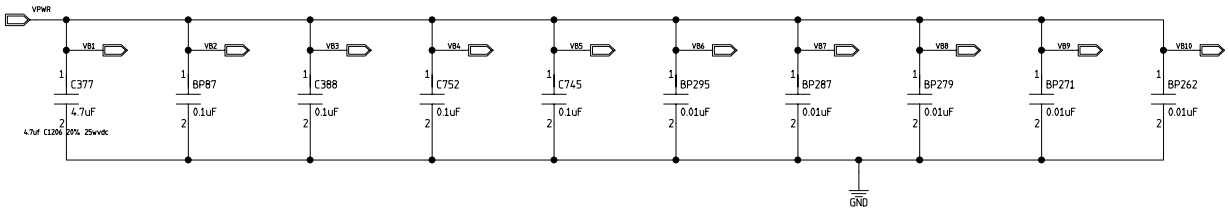

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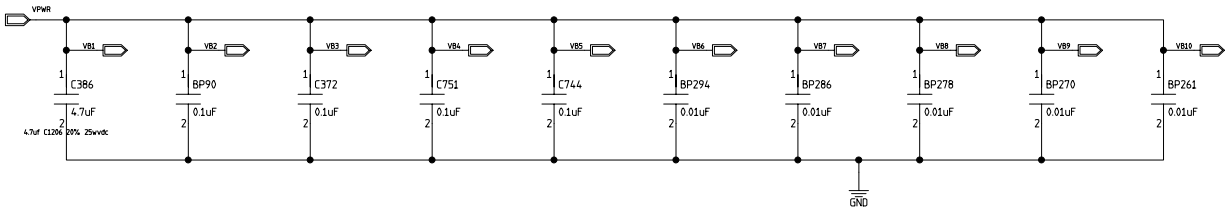

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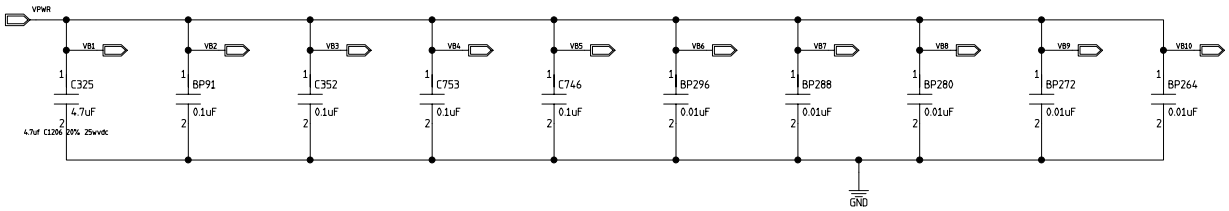

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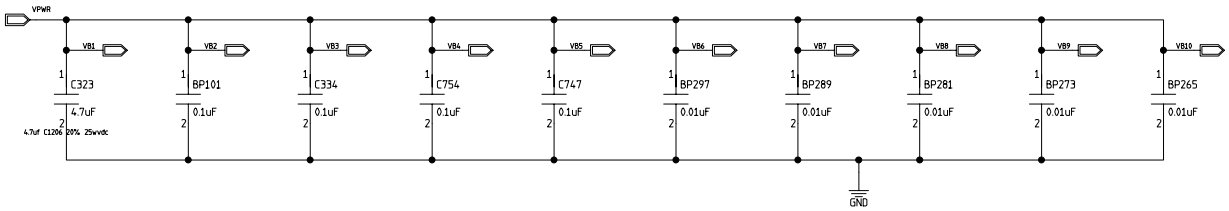

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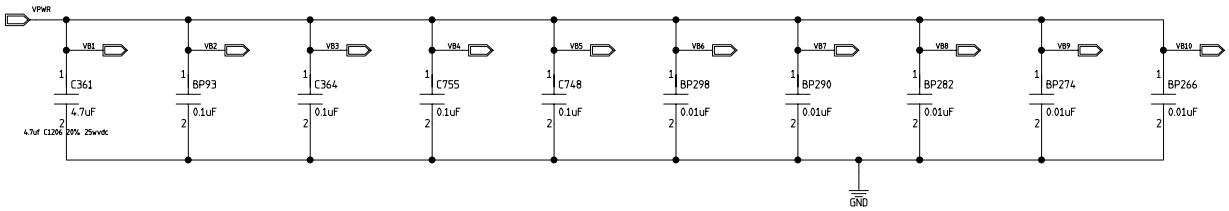

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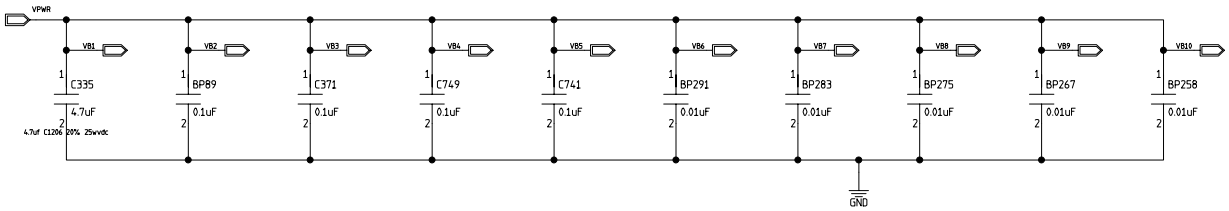

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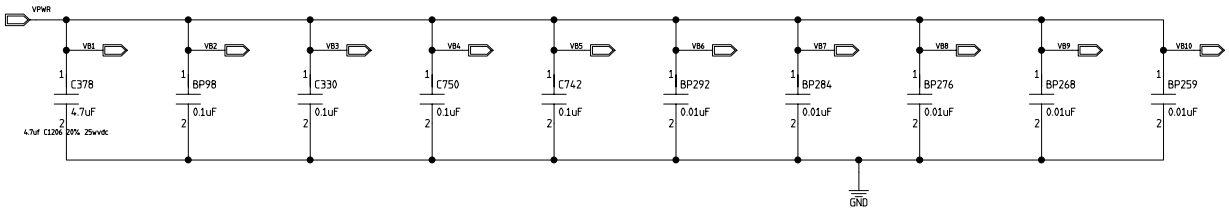

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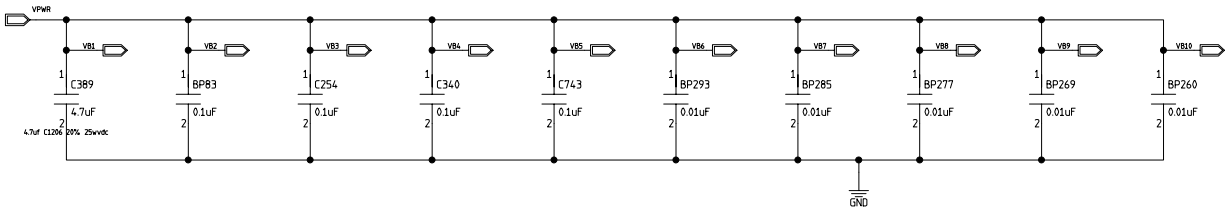

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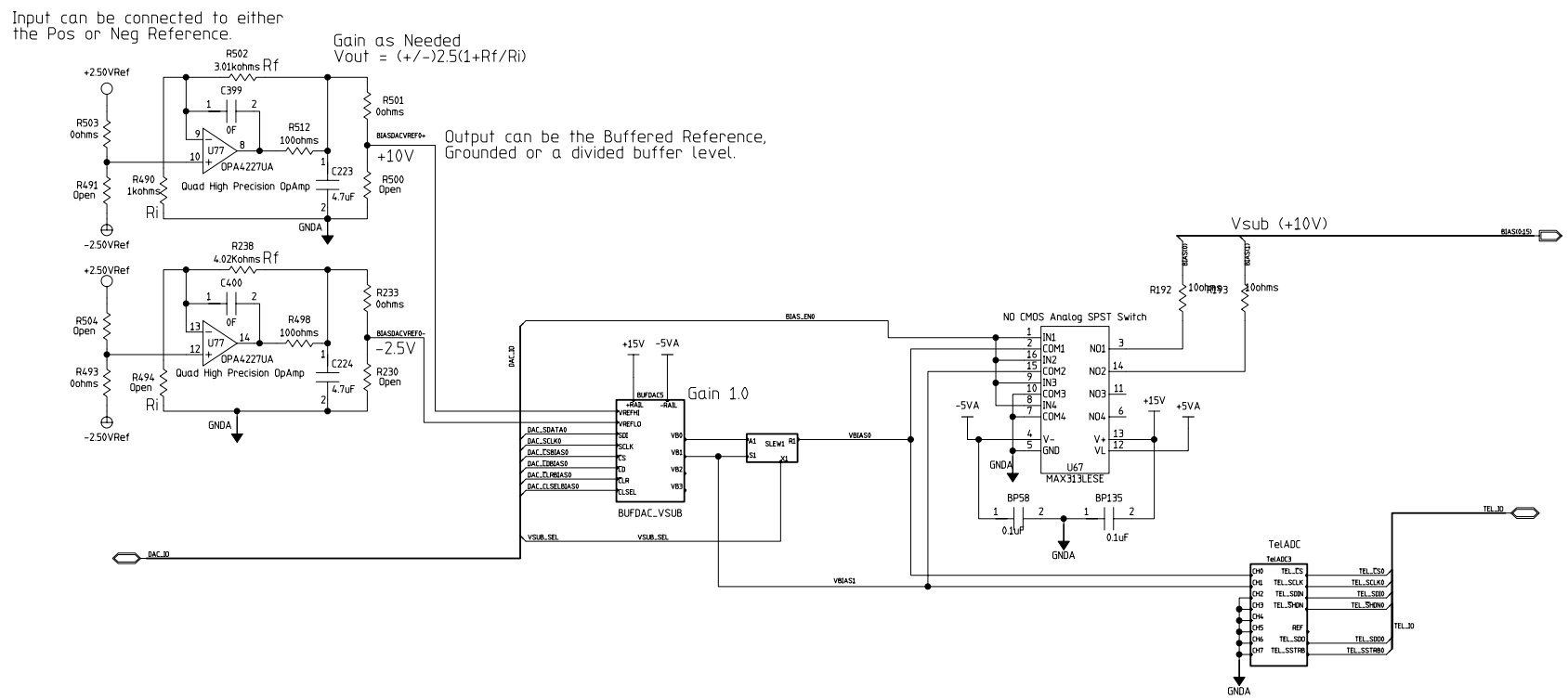

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Bias Output w/Enable 1-16

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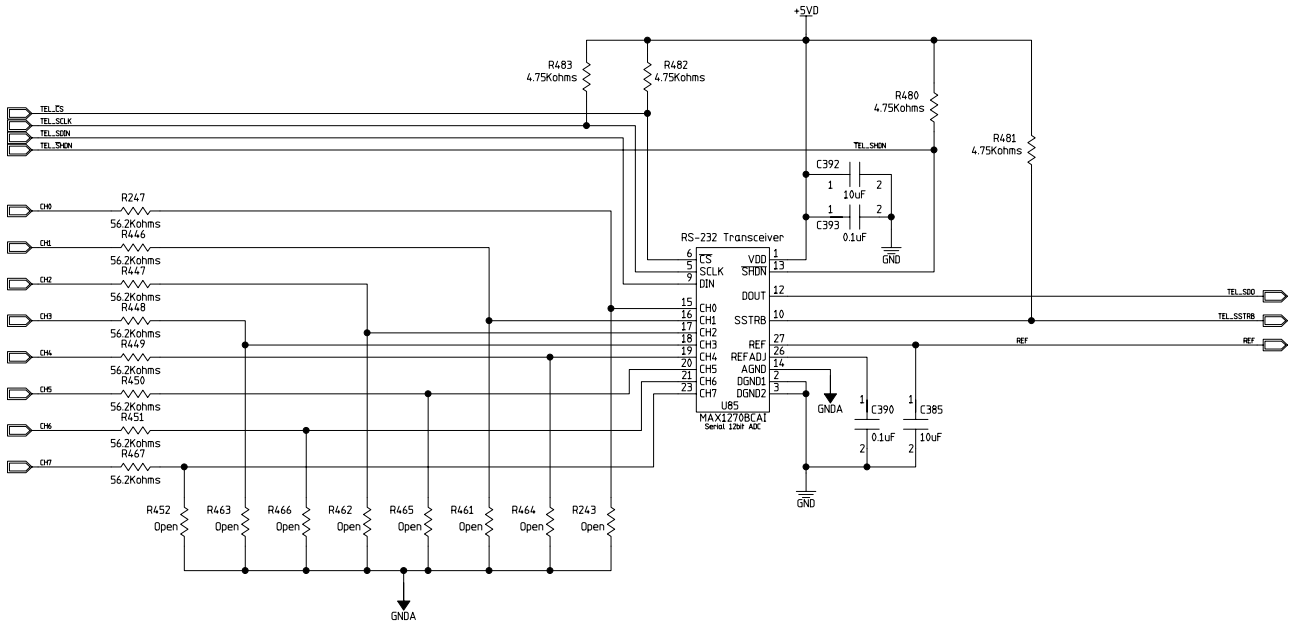

TELEMETRY CHANNELS BIAS 0-7

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8-Channel Telemetry ADC

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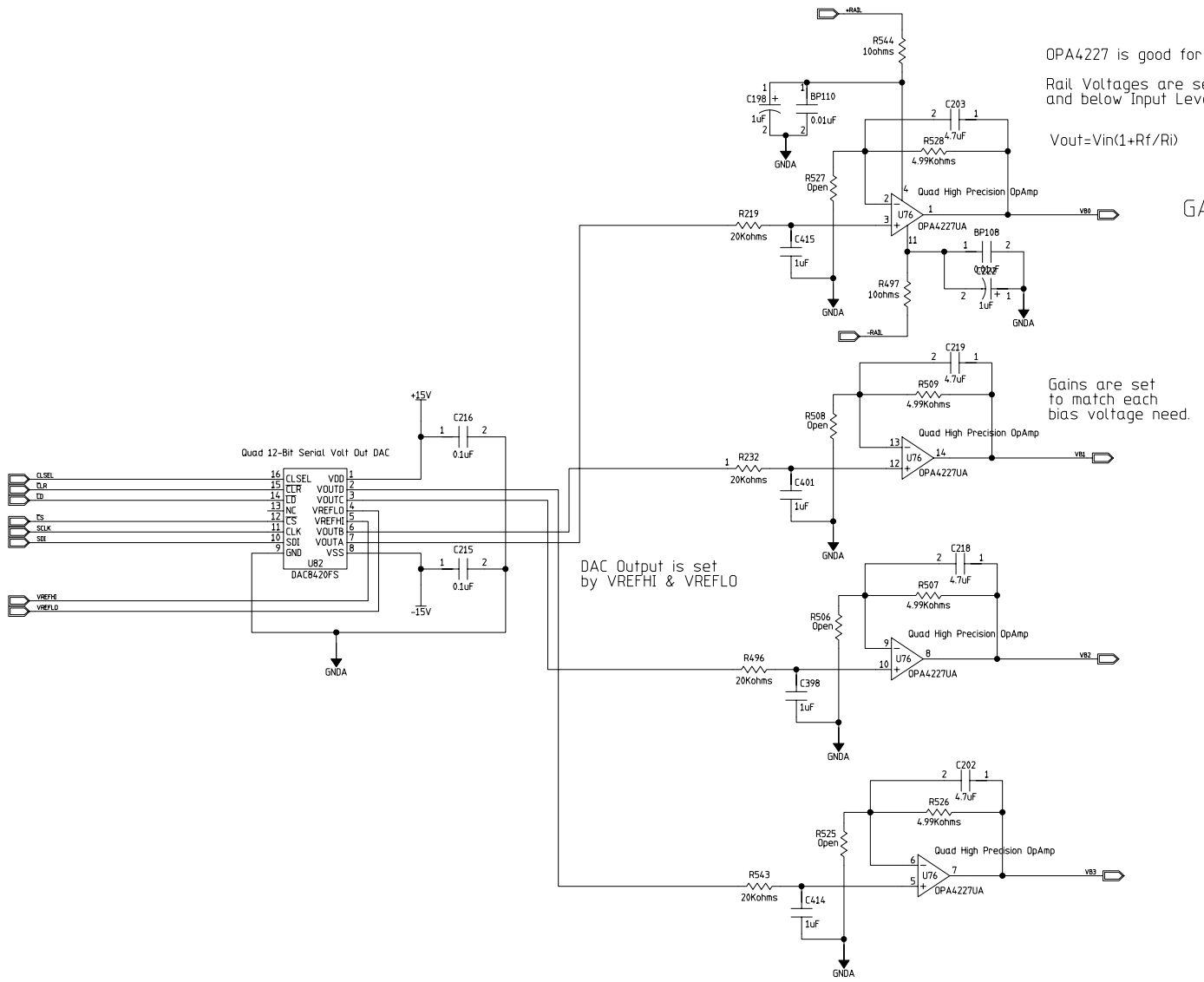

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4 Channel Buffered DAC - VSUB Ramp Control
BIAS 0,1

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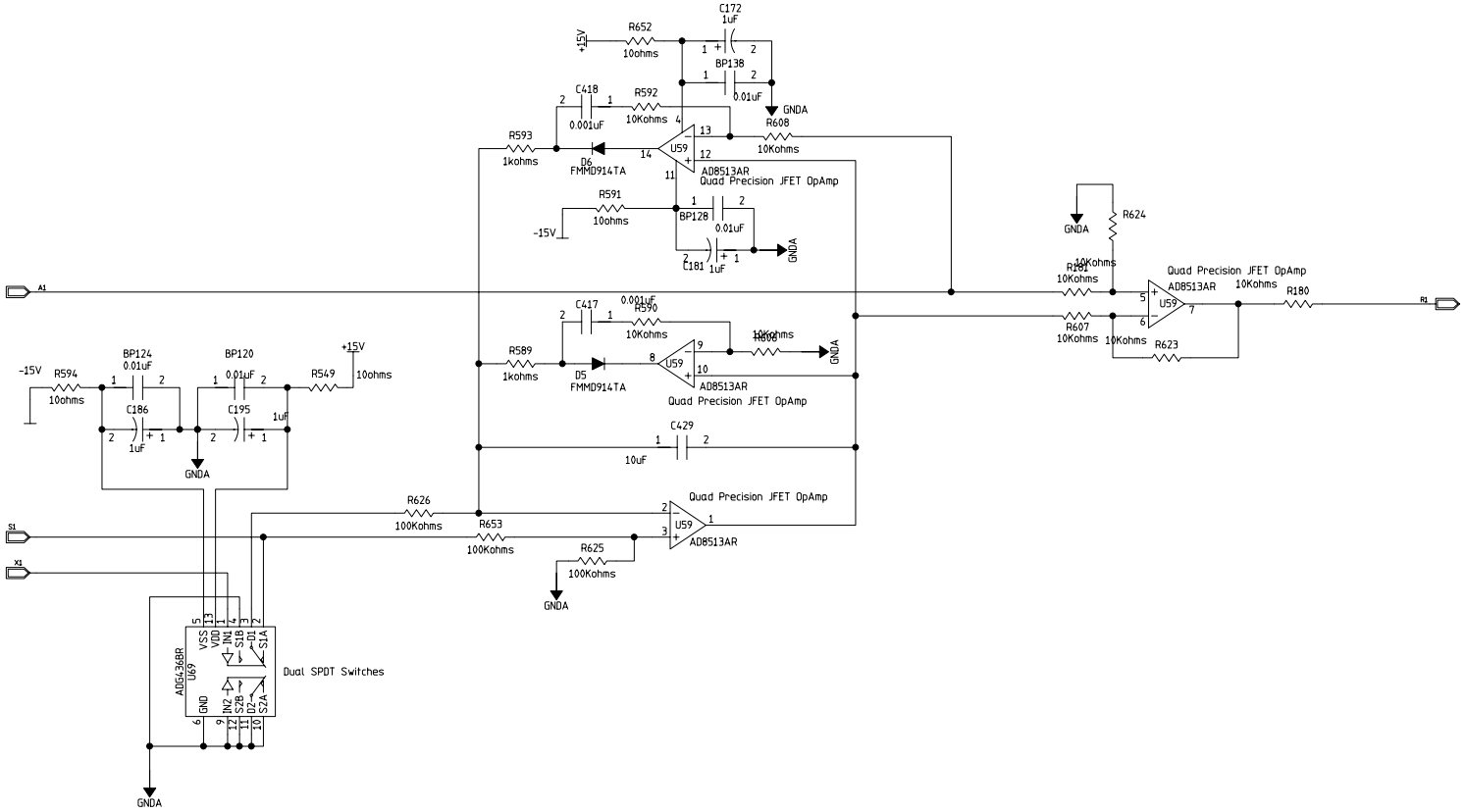
H=BND: V=4LA



MODIFIED 9/20/2006 10:54:27 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 17	DRAWN	David Huffman	DATE Nov. 3, 2005
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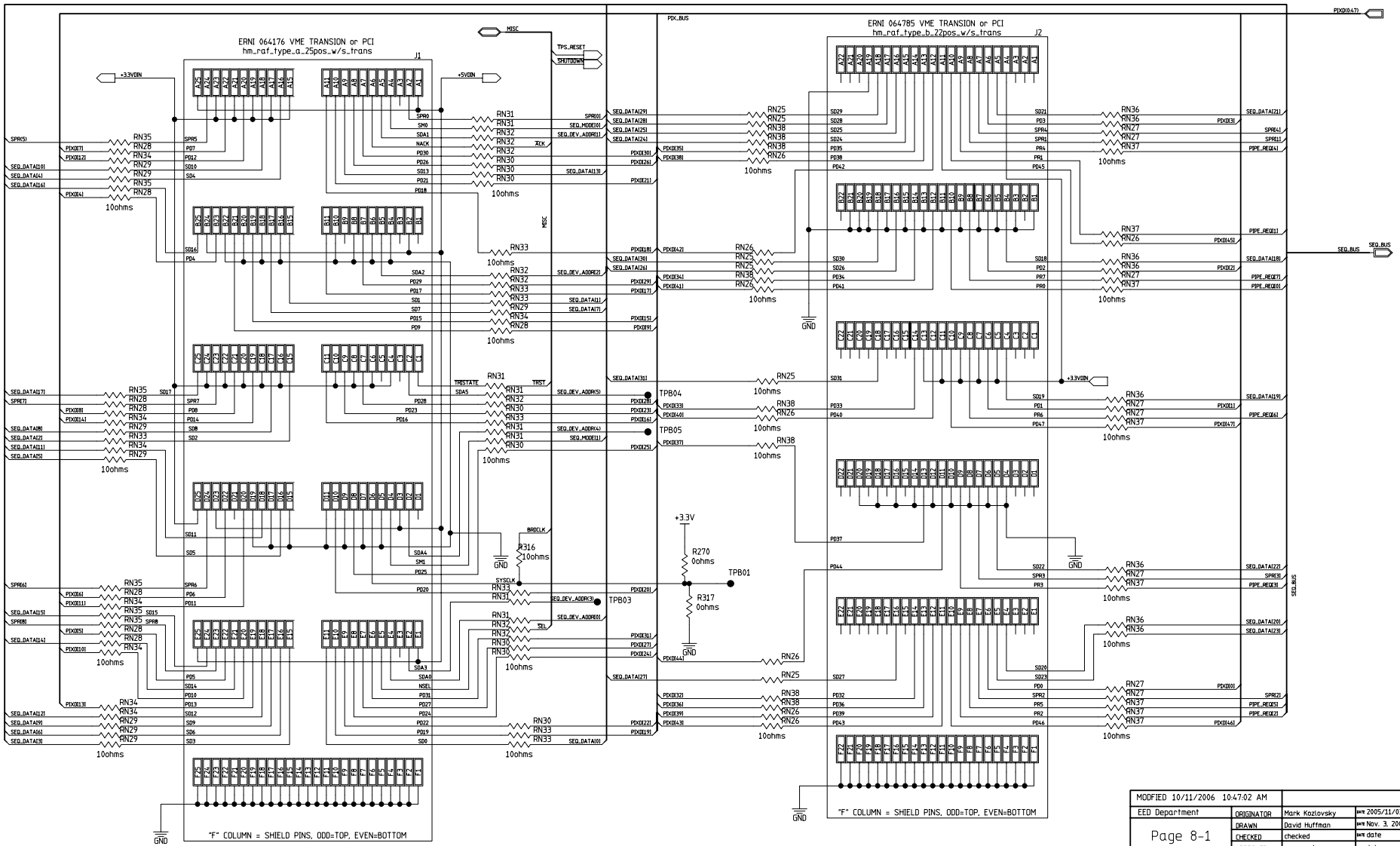
SLEW CONTROL

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=END: V=4LA



MODIFIED 10/11/2006 10:47:02 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 8-1	DRAWN	David Huffman	DATE Nov. 3, 2005
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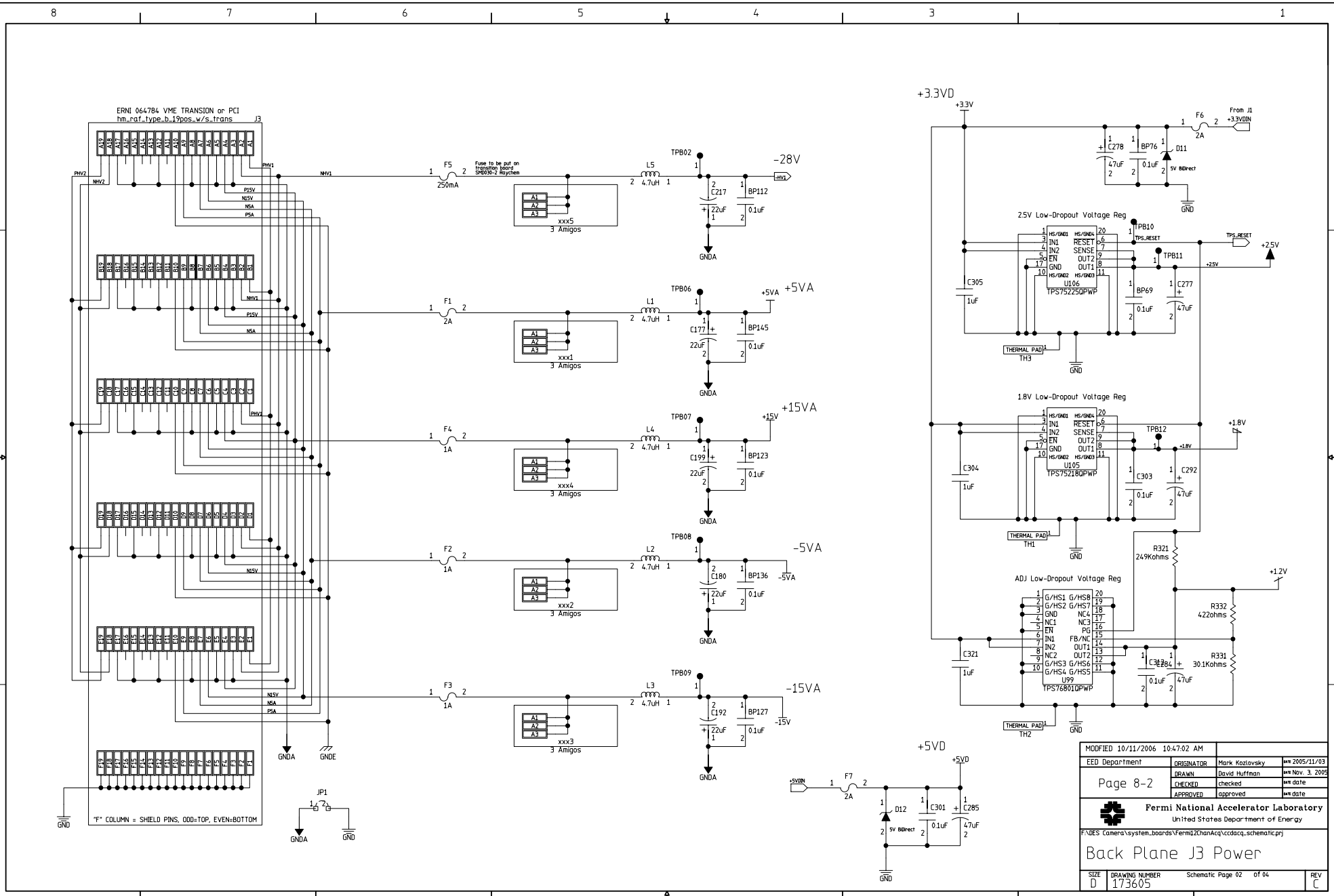
Back Plane J1 J2

SIZE	DRAWING NUMBER	Schematic Page 01 of 04	REV
D	173605		C

H=BND: V=4LA


ERNI 064784 VME TRANSION or PCI
hm_raf_type_b_19pos_w/s_trans
J3
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
F5
250mA
Fuse to be put on transition board SMD030-2 Raychem
L5
4.7uH
TPB02
-28V
-HV1
C217
22uF
BP112
0.1uF
xxx5
3 Amigos
F1
2A
L1
4.7uH
TPB06
+5VA
C177
22uF
BP145
0.1uF
xxx1
3 Amigos
F4
1A
L4
4.7uH
TPB07
+15VA
C199
22uF
BP123
0.1uF
xxx4
3 Amigos
F2
1A
L2
4.7uH
TPB08
-5VA
C180
22uF
BP136
0.1uF
xxx2
3 Amigos
F3
1A
L3
4.7uH
TPB09
-15VA
C192
22uF
BP127
0.1uF
xxx3
3 Amigos
GNDA
GNDE
GND
JP1
+3.3VD
+3.3V
From J1
+3.3VDIN
F6
2A
C278
47uF
BP76
0.1uF
D11
5V BDirect
2.5V Low-Dropout Voltage Reg
U106
TPS75225QPWP
TPB10
TPS_RESET
TPB11
+2.5V
C305
1uF
BP69
0.1uF
C277
47uF
THERMAL PAD
TH3
1.8V Low-Dropout Voltage Reg
U105
TPS75218QPWP
TPB12
+1.8V
C304
1uF
C303
0.1uF
C292
47uF
TH1
R321
249Kohms
+1.2V
ADJ Low-Dropout Voltage Reg
U99
TPS76801QPWP
R332
422ohms
R331
30.1Kohms
C321
1uF
C348
0.1uF
C284
47uF
TH2
+5VD
+5VDIN
F7
2A
D12
5V BDirect
C301
0.1uF
C285
47uF
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EED Department
Page 8-2
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
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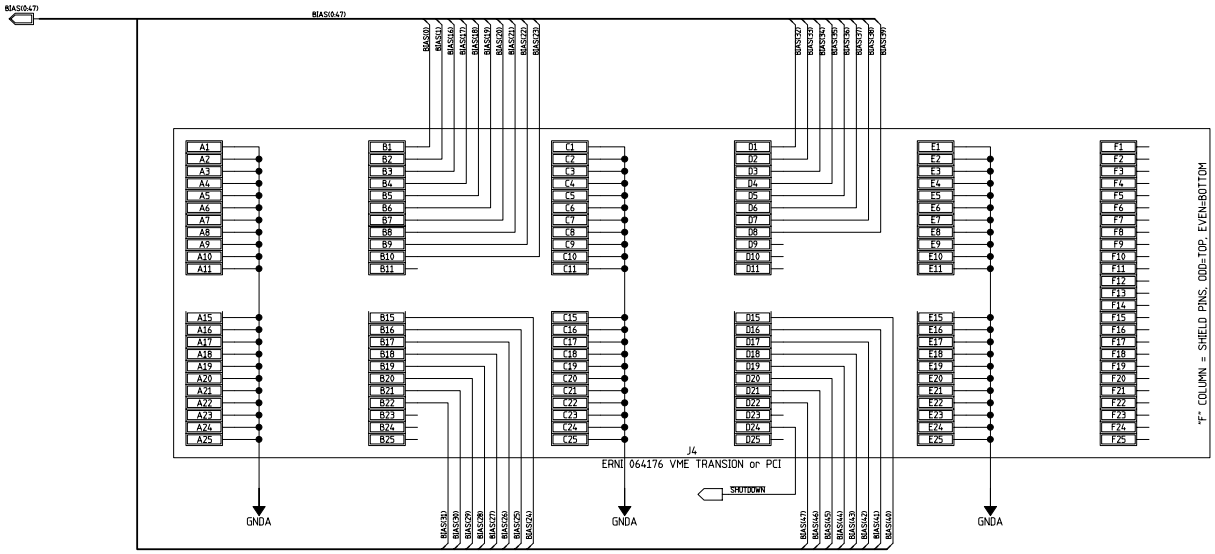
Back Plane J3 Power
SIZE D
DRAWING NUMBER 173605
Schematic Page 02 of 04
REV C



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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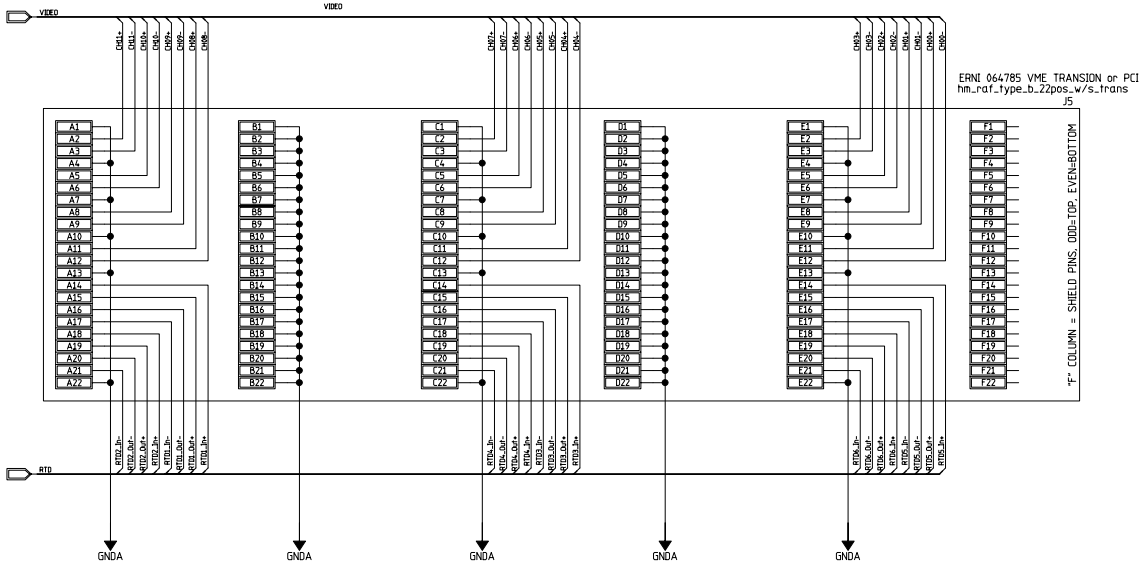
DIGITAL OUTPUTS & BIAS J4

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 03 of 04	C

H=GND, V=+LA



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 8-4	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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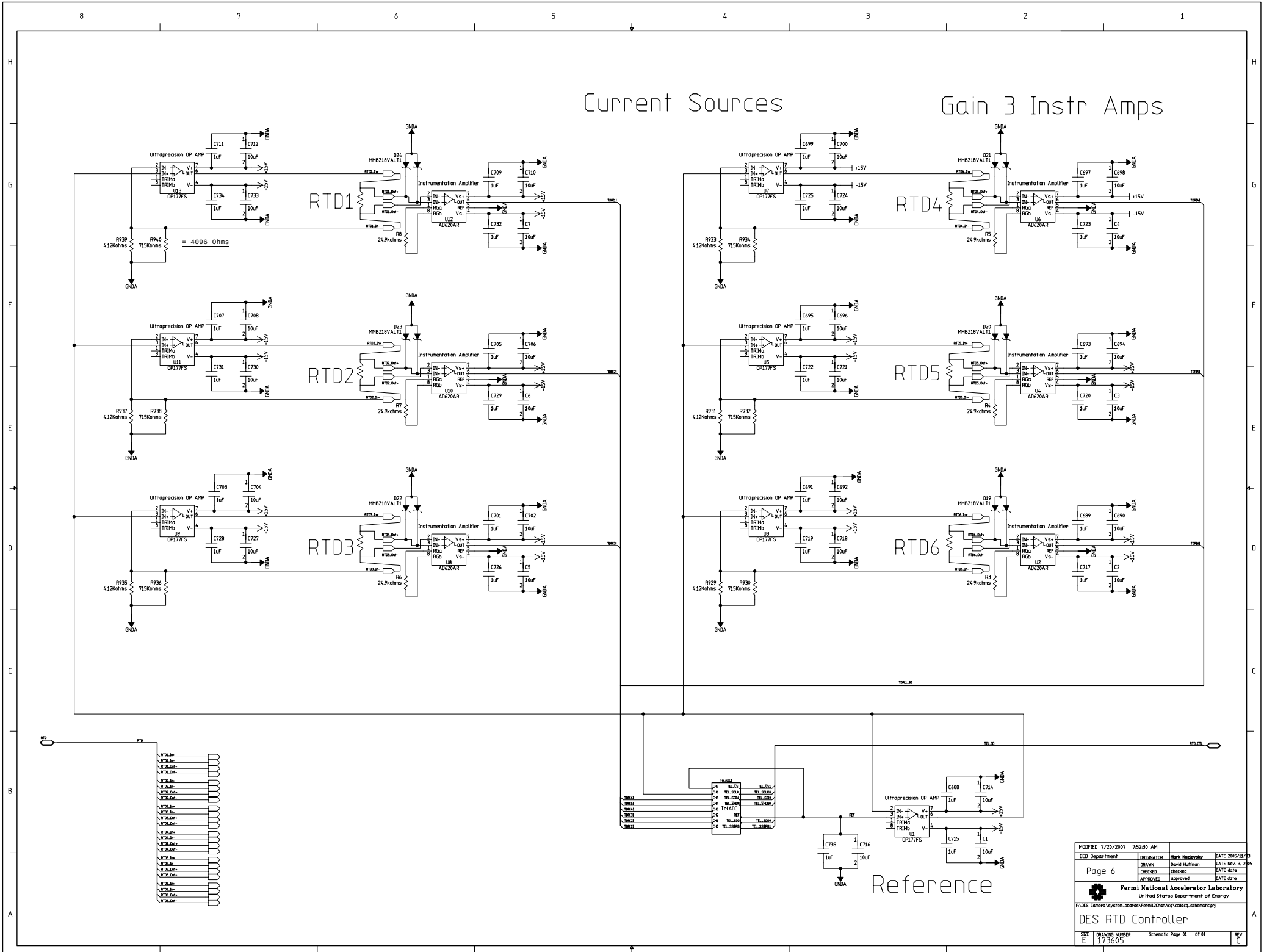
VIDEO INPUTS & RTD INPUTS J5

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 04 of 04	C

H=END: V=4LA


Current Sources
Gain 3 Instr Amps
RTD1
RTD2
RTD3
RTD4
RTD5
RTD6
Ultraprecision OP AMP
Instrumentation Amplifier
MMBZ18VALT1
AD620AR
OP177FS
= 4096 Ohms
Reference
MODIFIED 7/20/2007 7:52:30 AM
EED Department
Page 6
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
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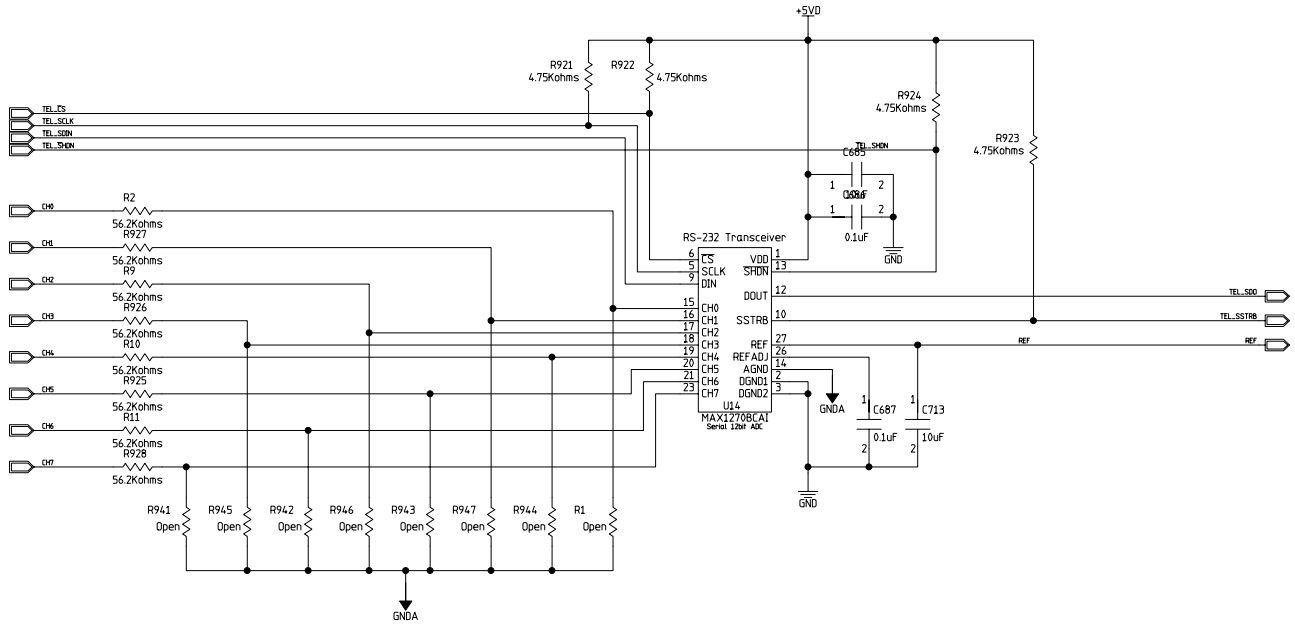
DES RTD Controller
SIZE E
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



RTD ADCs

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	APPROVED	approved	DATE date

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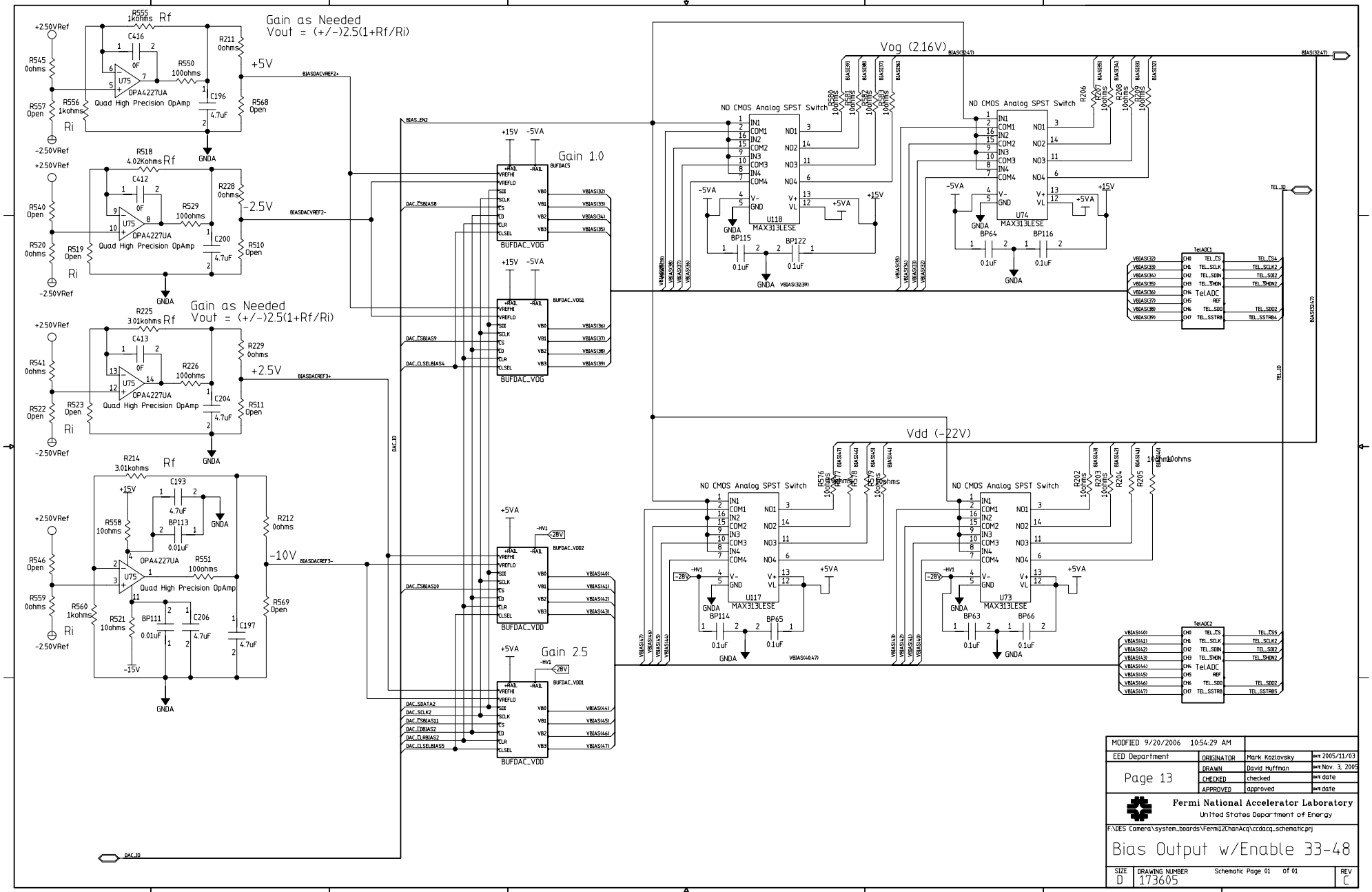
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA


Gain as Needed
Vout = (+/-)2.5(1+Rf/Ri)
Gain as Needed
Vout = (+/-)2.5(1+Rf/Ri)
Vog (2.16V)
Vdd (-22V)
Gain 1.0
Gain 2.5
Quad High Precision OpAmp
OPA4227UA
NO CMOS Analog SPST Switch
MAX313LESE
BUFDAC_VOG
BUFDAC_VDD
TelADC
+2.50VRef
-2.50VRef
+5V
-2.5V
+2.5V
-10V
+15V
-15V
-5VA
+5VA
GNDA
BIASDACVREF2+
BIASDACVREF2-
BIASDACREF3+
BIASDACREF3-
BIAS(32:47)
TEL_ID
DAC_ID
MODIFIED 9/20/2006 10:54:29 AM
EED Department
Page 13
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Nov. 3, 2005
CHECKED checked date
APPROVED approved date
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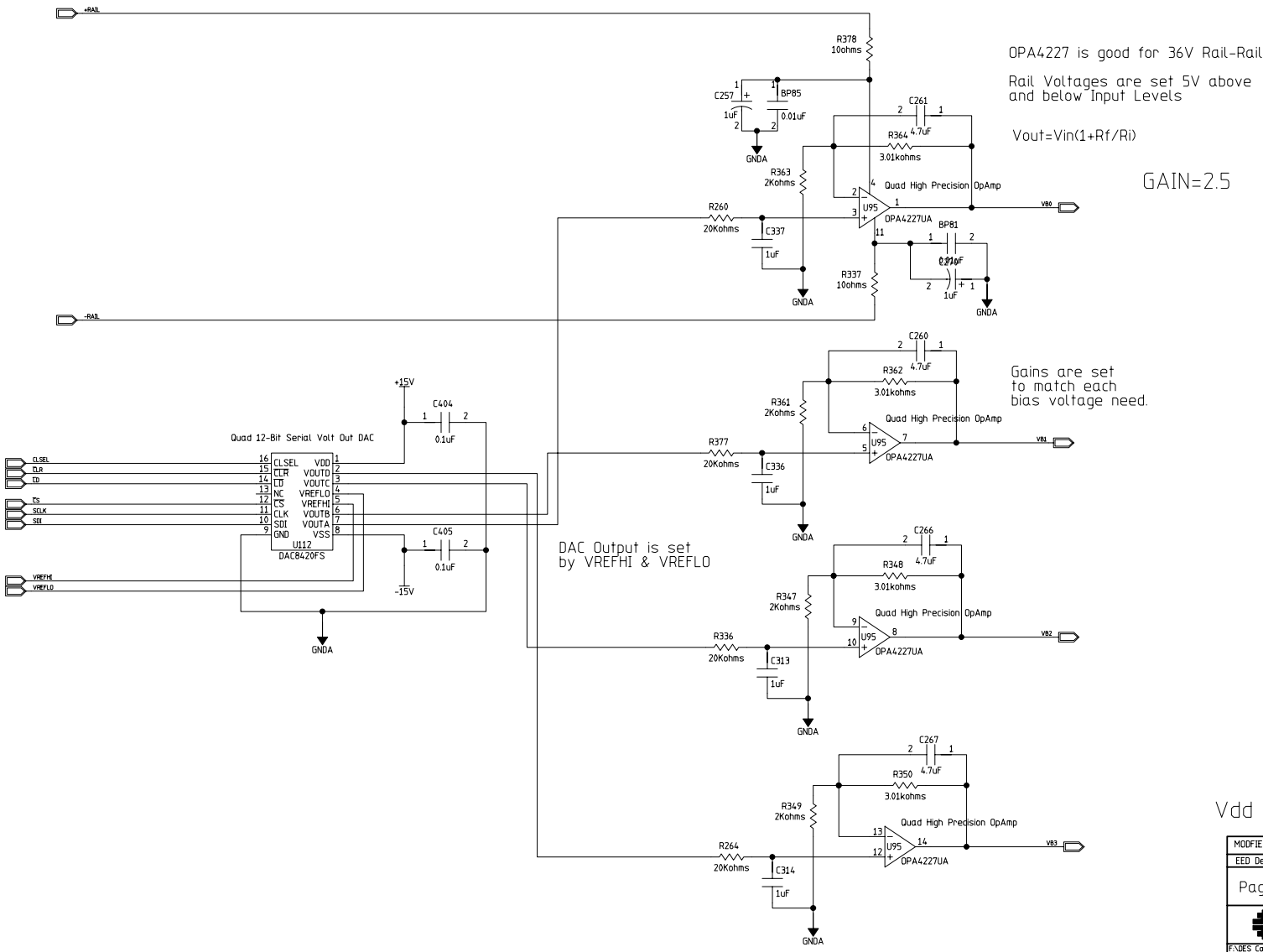
Bias Output w/Enable 33-48
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=2.5

Gains are set
to match each
bias voltage need.

Vdd BIAS CHANNELS 40-43

MODFIED 5/24/2006 12:34:00 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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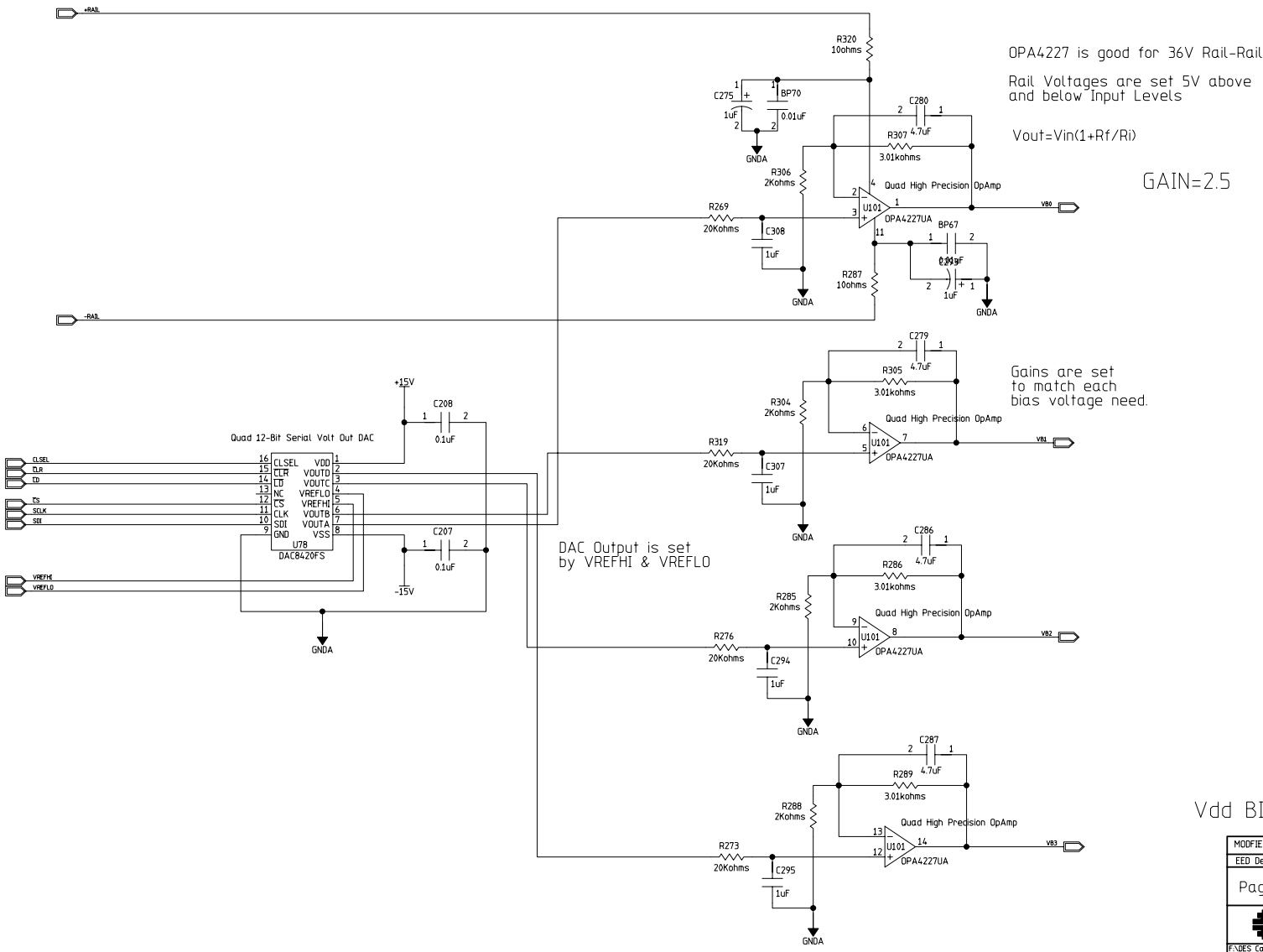
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=2.5

Gains are set to match each bias voltage need.

DAC Output is set by VREFHI & VREFLO

Vdd BIAS CHANNELS 44-47

MODFIED 5/24/2006 12:34:00 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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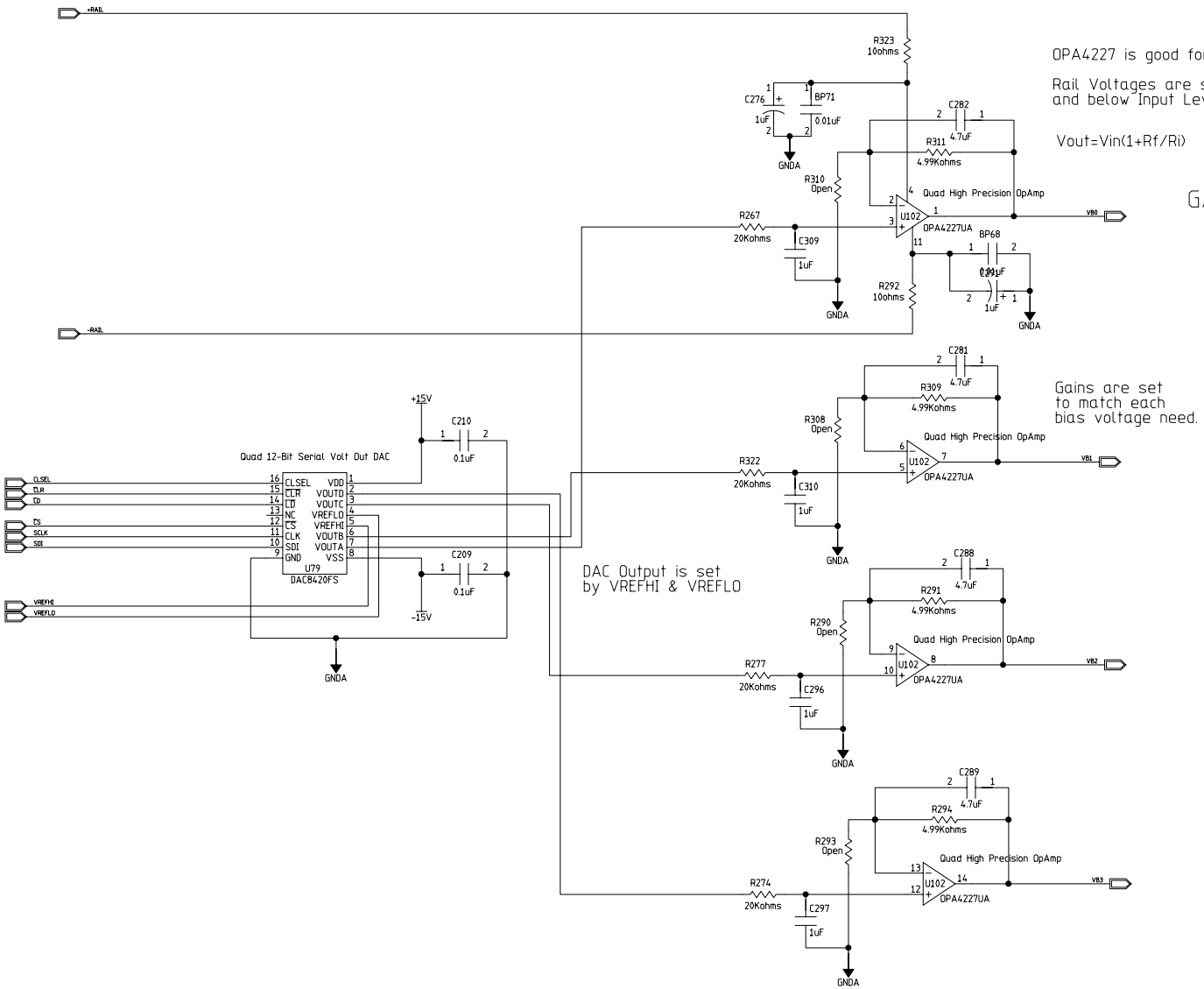
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA


+RAIL
-RAIL
R323
10ohms
C276
1uF
BP71
0.01uF
GNDA
C282
4.7uF
R311
4.99Kohms
R310
Open
Quad High Precision OpAmp
U102
OPA4227UA
VB0
R267
20Kohms
C309
1uF
BP68
0.01uF
1uF
R292
10ohms
C281
4.7uF
R309
4.99Kohms
R308
Open
VB1
R322
20Kohms
C310
1uF
C288
4.7uF
R291
4.99Kohms
R290
Open
VB2
R277
20Kohms
C296
1uF
C289
4.7uF
R294
4.99Kohms
R293
Open
VB3
R274
20Kohms
C297
1uF
+15V
C210
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
TLR
TD
CS
SCLK
SDI
VREFHI
VREFLO
CLSEL
CLR
TD
NC
CS
CLK
SDI
GND
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
U79
DAC8420FS
C209
0.1uF
-15V
DAC Output is set
by VREFHI & VREFLO
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.0
Gains are set
to match each
bias voltage need.
Vog BIAS CHANNELS 36-39
MODIFIED 5/24/2006 12:32:22 PM
EED Department
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
Page 10 -9
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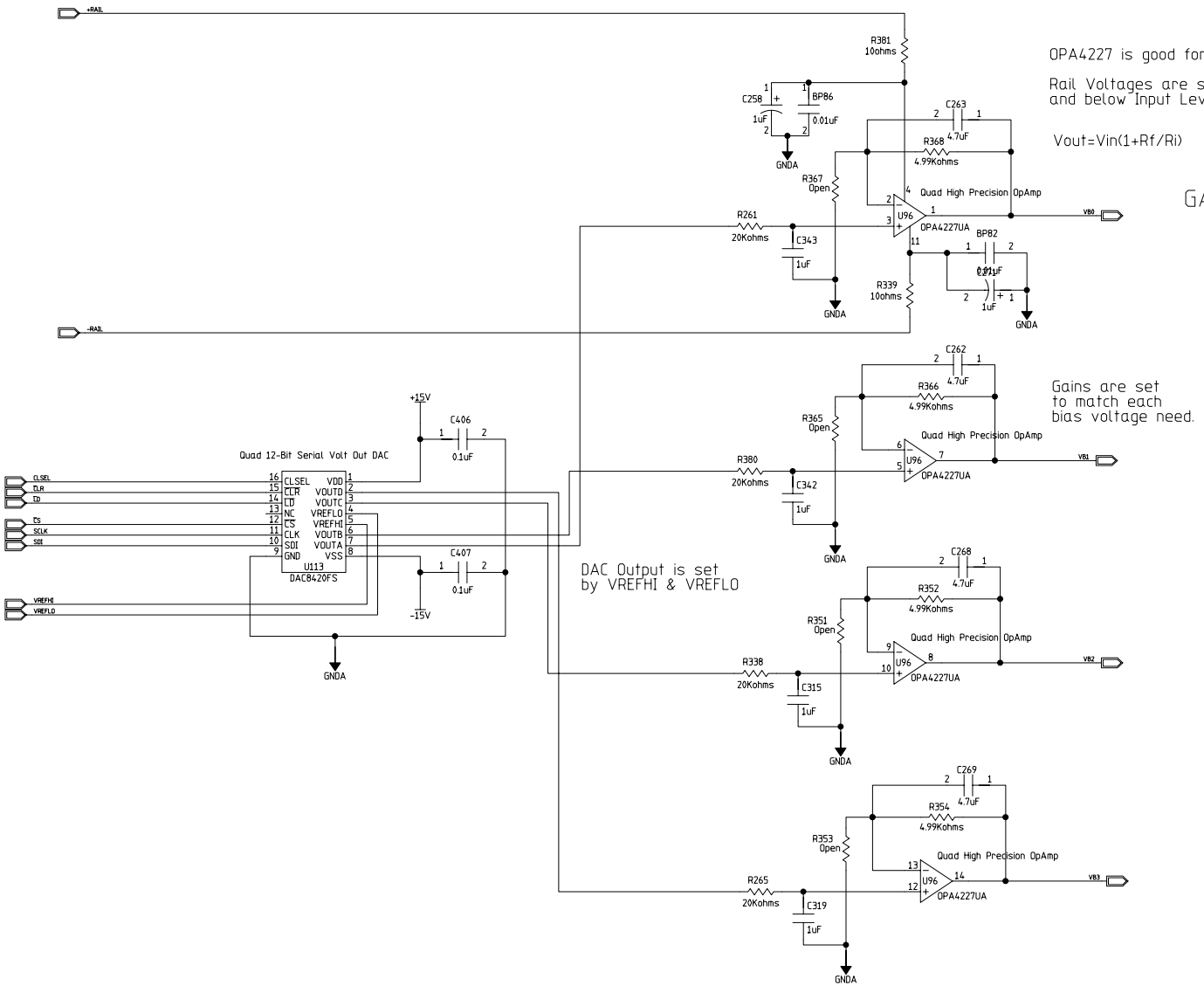
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
4 Channel Buffer DAC - Vog
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.0

Gains are set to match each bias voltage need.

DAC Output is set by VREFHI & VREFLO

Vog BIAS CHANNELS 32-35

MODFIED 5/24/2006 12:32:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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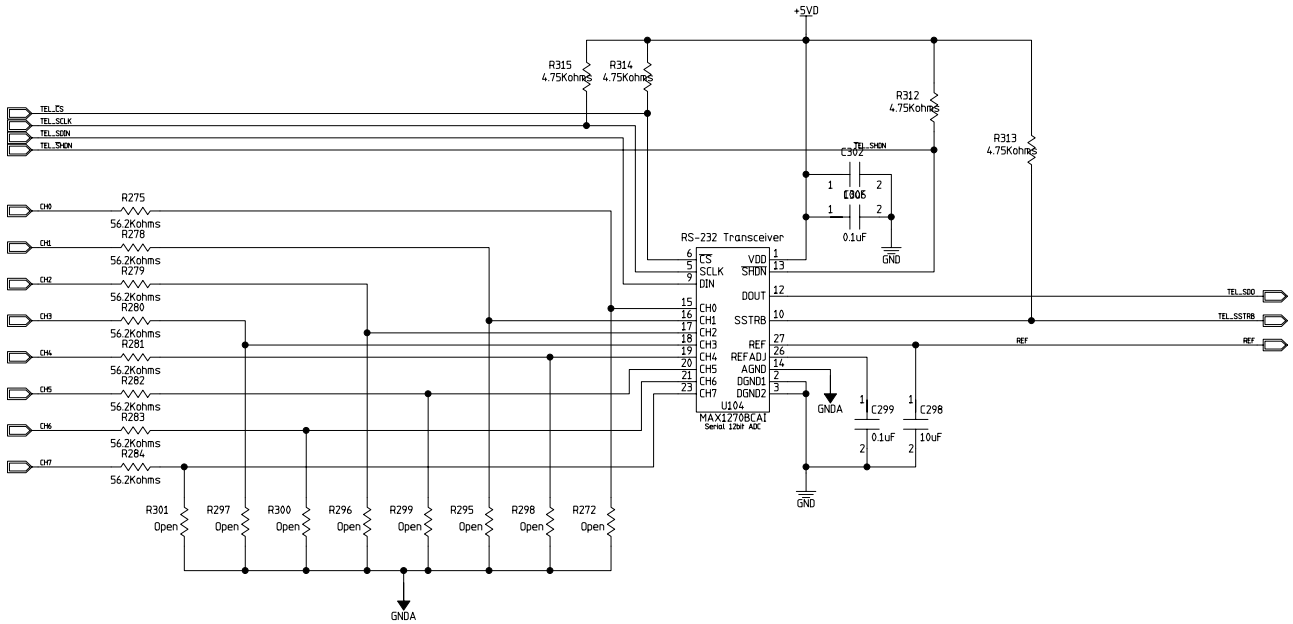
4 Channel Buffer DAC - Vog

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 40-47

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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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	APPROVED	approved	DATE date

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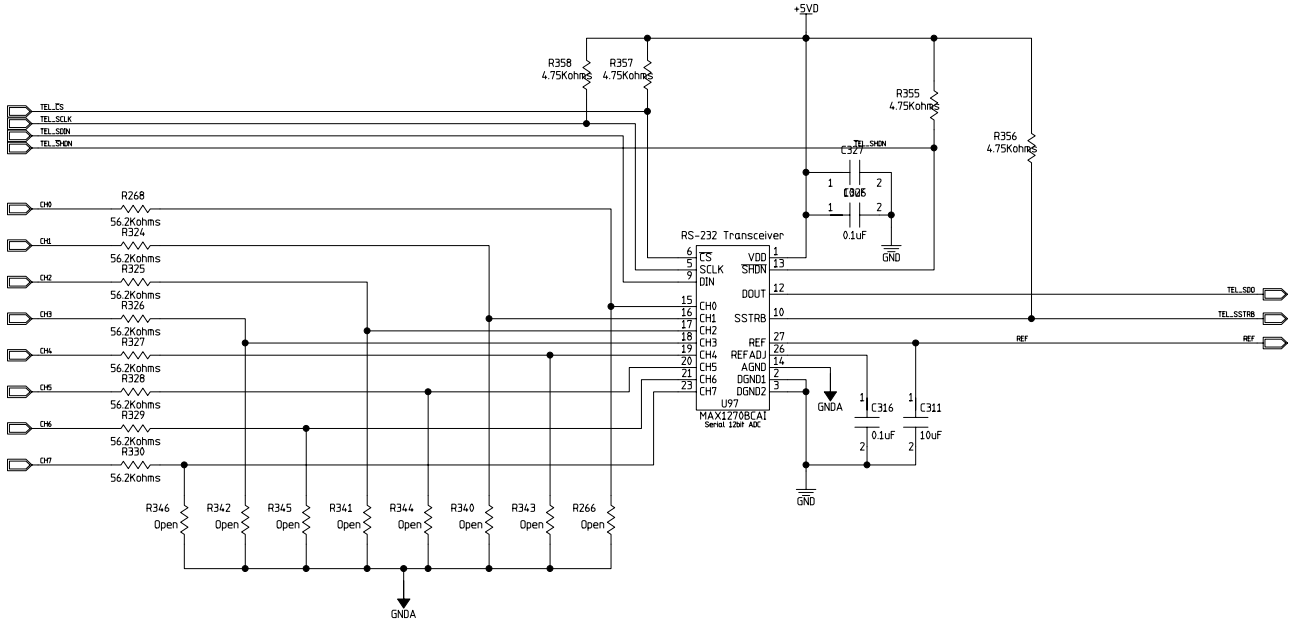
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 32-39

MODIFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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	APPROVED	approved	DATE date

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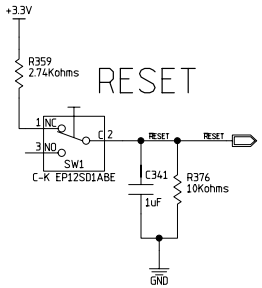
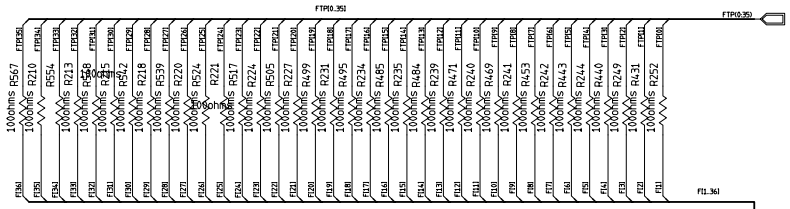
8-Channel Telemetry ADC

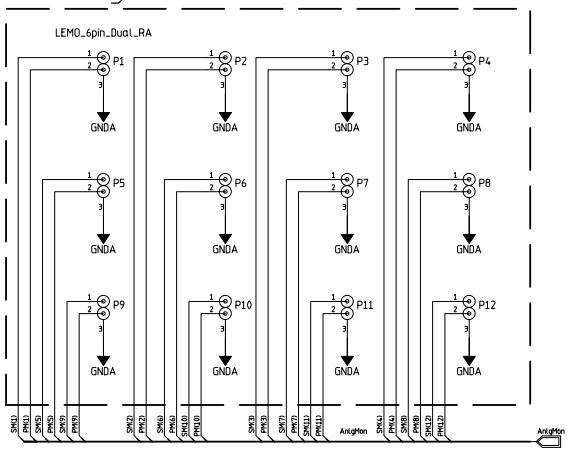
SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA





Analog Test Points



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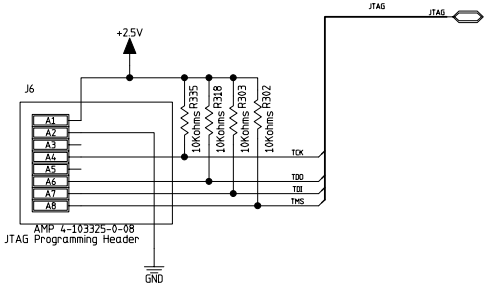
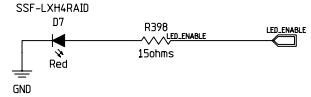
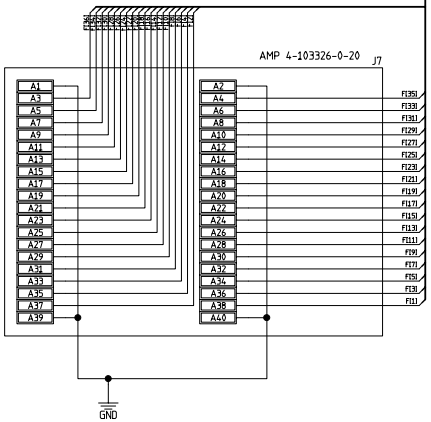


STATUS



Digital Test Points



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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J6 Test Points/ Analog Mon
J7 JTAG

SIZE	DRAWING NUMBER		REV
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H=BND: V=4LA