

LBL small CCD Operating Procedures

CCD Voltages

Typical voltages for LBL CCDs are:

| Signal | Signal name | Typical Voltage | Notes |
|-------------------|--------------------------|-----------------|---|
| Substrate Bias | Vsub | 40V-80V | Optimum performance at highest voltage, possible breakdown at higher voltages. Use high impedance supply (>10 kohm). Use Vsub=0V during persistent image erase. |
| Output Drain | Vdd | -22V | Low gain below -20V, transistor glow, breakdown above -25V |
| Reset Drain | Vr | -12.5V | Sets the output working point. Use Vr and Vog to prevent charge injection. |
| Output Gate | Vog | 2.16 V | Prevents charge injection. Adjust in conjunction with Vr if necessary. If Vog is too high serial CTE is compromised. |
| Vertical Clocks | V1,V2,V3, FS1,FS2,FS3 | +5V -3V | Increase high side to +6V to erase persistent image |
| Transfer Gate | Tg | +5V -3V | If parallel CTE is compromised try adjusting Tg first. |
| Horizontal Clocks | H1,H2,H3 | +6V -4V | |
| Summing Well | SW | +5V -5V | |

P+ guard is grounded, N+ guard is not connected, except during persistent image erase, when it is grounded.

The video output signal will be at about -18V if driving a 20 kOhm DC load to ground. Noise seems to be lowest if the AC coupled load is minimal (>200 kOhm). The combined load should be between 15 and 20 kOhm.

We use a two-stage inverting preamplifier mounted at the dewar exit to obtain the required signal polarity for the GenII controller, while the high input impedance is maintained. The inverting output stage can easily drive a shielded cable connected to the GenII video input without compromising the settling time of the signal.

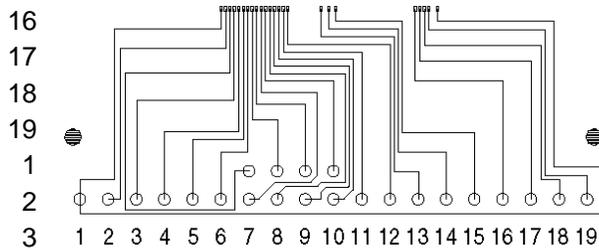
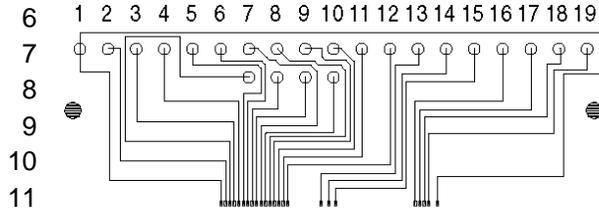
CCD Bond Pads

| | | |
|----------|----|--|
| V sub | 1 | The LBL CCDs have two readout transistors. Each transistor |
| H1 U | 2 | and it's respective half of the serial register along with one |
| H2 U | 3 | copy of all parallel signals is brought out on 20 bond pads on |
| H3 U | 4 | one side of the chip (see table on left). |
| V r U | 5 | |
| RG U | 6 | When looking at the bond-pad side of the CCD with the serial |
| Video U | 7 | register (many bond pads) on the left side the upper half of the |
| V dd U | 8 | CCD is referred to as the U-side, the lower half as the L-side. |
| V opg U | 9 | |
| SW U | 10 | |
| TG | 11 | |
| p+ guard | 12 | |
| FS1 | 13 | |
| FS2 | 14 | |
| FS3 | 15 | |
| V1 | 16 | |
| V2 | 17 | |
| V3 | 18 | |
| n+ guard | 19 | |
| V sub | 20 | |

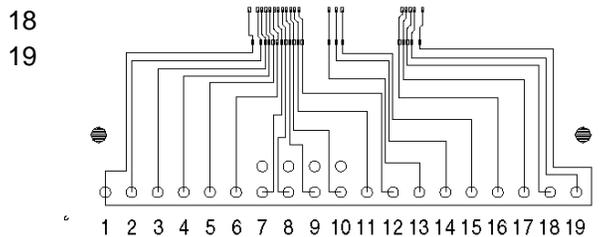
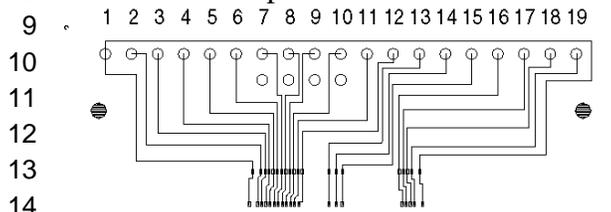
Connector Pinout:

V sub
 H1 U
 H2 U
 H3 U
 V r U
 RG U
 Video U
 V dd U
 V opg U
 SW U
 TG
 p+ guard
 FS1
 FS2
 FS3
 V1
 V2
 V3
 n+ guard
 V sub
 H1 L
 H2 L
 H3 L
 V r L
 RG L
 Video L
 V dd L
 V opg L
 SW L
 TG
 p+ guard
 FS1
 FS2
 FS3
 V1
 V2
 V3
 n+ guard

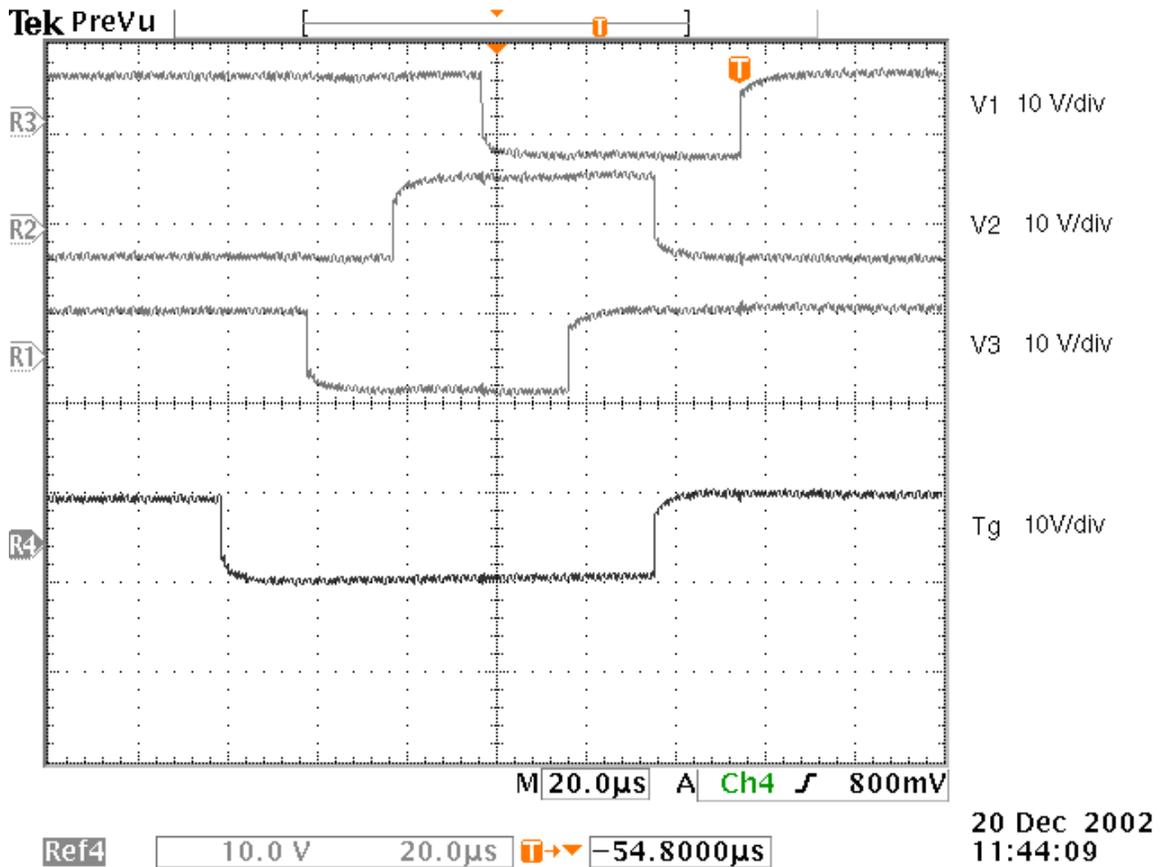
1 Here is the pinout of the two connector rows on the CCD
 2 package.
 3 Below is the pin assignment as seen from the front of a back
 4 illuminated device.



5 Below is the circuit of the other side for reference. This is the
 6 front side for a front illuminated device. The orientation can be
 7 easily verified by observing the asymmetrical arrangement of
 8 the 4 additional pins.



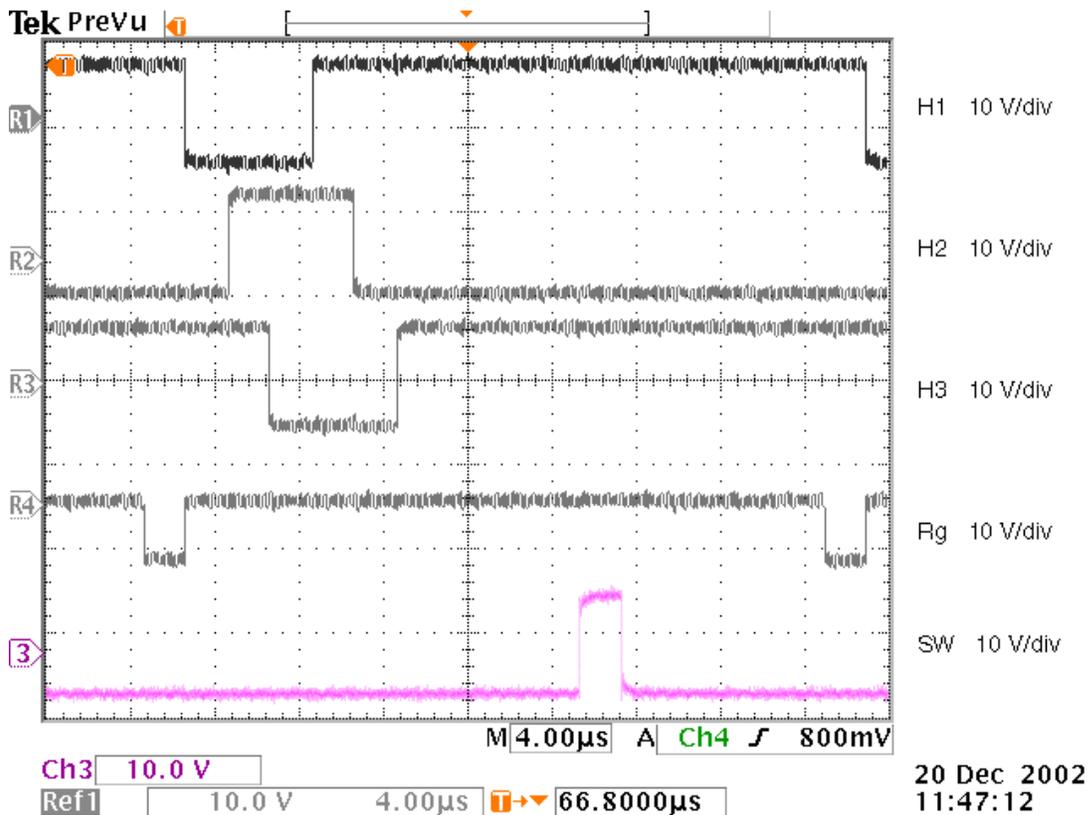
Typical Waveforms



Parallel waveforms for slow clocking with 20 us overlap. Overlap can be reduced below 10 us to increase readout speed if wiring between drivers and CCD is short enough.

We typically connect FS1 to V1, FS2 to V2, FS3 to V3 to read out the entire chip. If the Frame Store functionality is desired the image can be transferred from the imaging area (V1,2,3) to the frame store area (FS1,2,3), then the frame store area can be read out while the imaging area is exposed to a new image. Naturally this reduces the usable chip size by half.

During integration phases 1 and 2 should be low.



Serial clock waveforms for 30 kHz readout to the L transistor.

Note that H1 and H3 are symmetrical around H2, so swapping of H1 and H2 reverses the clocking direction in the serial register, enabling readout to the U transistor.

If the horizontals on the L side are clocked with the above pattern, while on the U side H1 and H3 are reversed the CCD is read out to both transistors simultaneously.

Reduction of the clock overlap, settling and integration times can increase readout speed to 100 kHz with modest noise gains.

The serial clock overlap as well as the reset low time can be reduced to 160 ns.

The summing well high time can be reduced to 500 ns.

The integration time can be reduced to 3760 ns (or below with increased read noise).

The settling time (between the last clock transition and the begin of integration) can be reduced to 120 ns.

These minimum values worked well in our system, but may not be optimal for your setup due to different cabling length, preamp input capacitance, and other parasitic capacitances.

Note however that the SDSU Gen II controller has problems at 100 kHz in the slow integration speed setting due to excessive impedance in the integration capacitor reset circuitry. The high-speed setting does not have those problems, but the higher gain in this setting will saturate the ADC below full well level.

See SDSU controller modification pages for options.

Persistent Image Erase

To erase persistent images, and to achieve ultimate dark current after initial power-up the CCD should be erased. Different procedures have been successfully used.

One option is to reduce the Substrate bias below 30V, then short N+ to ground, while driving the parallel clocks at +6V high level. It is important that the impedance of the substrate bias power supply is large enough to prevent a current of more than a few mA from flowing between V_{sub} and N+. If in doubt further reduce V_{sub} during the erase.

The second option does not require wiring of the N+ guard. During erase the substrate bias is clamped to ground while the parallel clocks are driven to +6V. This simpler procedure has been reported to work well, but we do not have extensive experience with the achievable level of dark current.