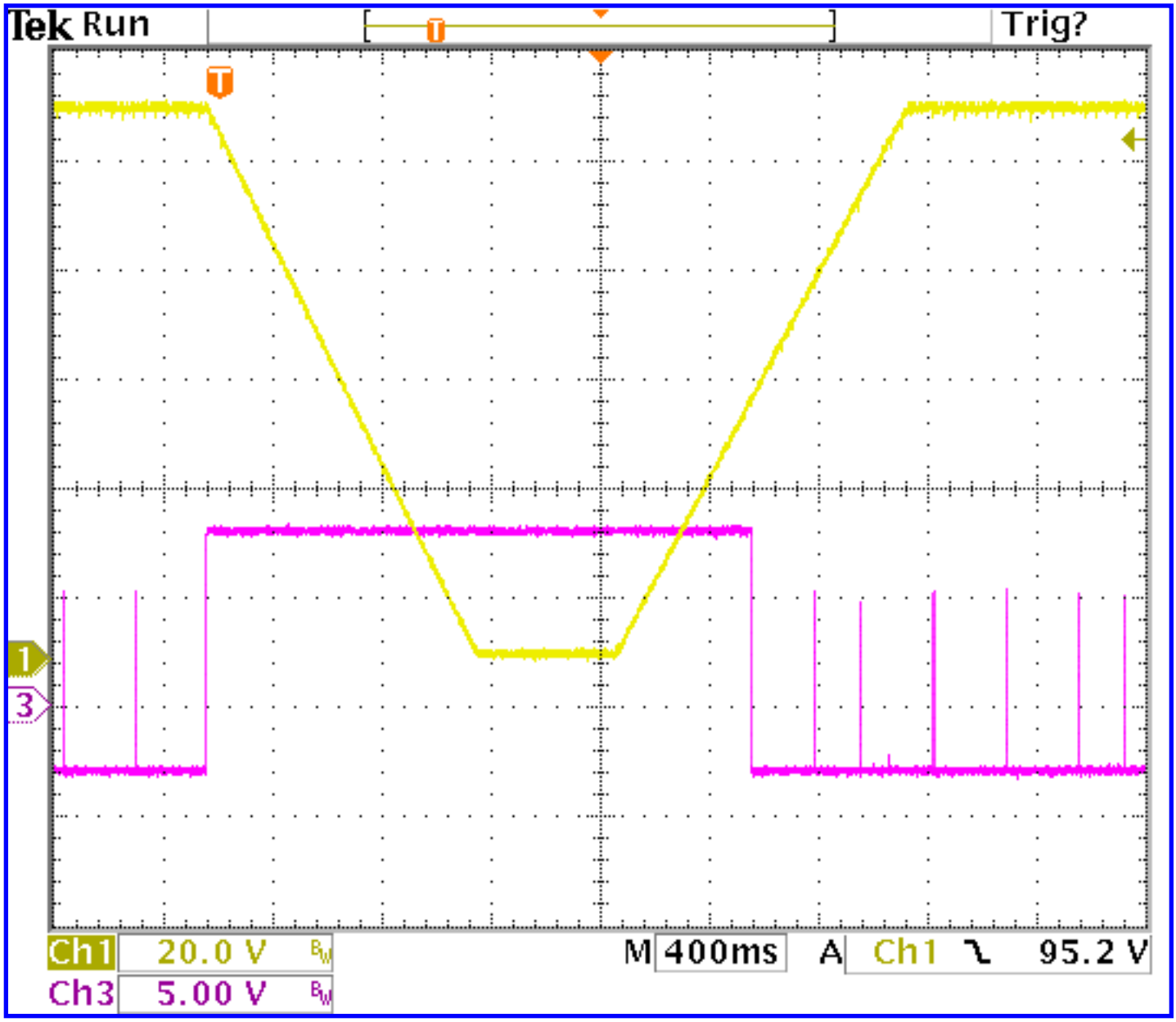
Persistent Image Erase Procedure

When CCDs are first turned on or subjected to strong, saturating illumination, residual •ghost• images or high dark current signals are produced. These are caused by the emptying of dielectric interface traps by the excess hole carriers produced by saturation. These traps then refill slowly at the low operating temperature by releasing holes into the wells in a process extending over many hours.

These effects can be eliminated by an •erase• procedure in which the traps are quickly filled with electrons. The current recommended procedure is as follows:

- Lower V_{sub} to 0 V in a controlled linear manner.
- Do *not* ground the n+ guard electrode.
- Increase all the parallel clocks to a value high enough to produce inversion and hold them at this value, experimentally found to be 3 to 5 V above barrier phase.
- After a brief delay (fraction of a second) ramp V_{sub} back to normal operating voltage
- We use a ramp rate of about 75 V/s.
- When V_{sub} b > 10 V restore the parallel clocks to normal values.

In order to implement the erase feature, we constructed a special V_{sub} regulator circuit which provides the linear ramp. A more detailed discussion of the erase procedure including a block diagram of the ramping circuit we use is given here The ramping circuit is controlled by our image acquisition program (Voodoo). The figure below shows an example waveform generated by the ramp circuit under program control.



In the figure the V_{sub} ramp is shown in yellow and the parallel clocks in magenta. During the erase period all parallel clocks are held high at +8 V and during regular clocking go between +5 V and •3 V.

After the erase, any persistent ghost images should be removed and dark current should be reduced to a minimum.

Improved Erase Technique for LBNL CCDs

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Introduction

- When CCDs are first turned on or subjected to strong, saturating illumination, residual "ghost" images or high dark current signals are produced. These are caused by the emptying of dielectric interface traps by the excess hole carriers produced by saturation. Traps refill slowly by releasing holes into the wells in a process extending over hours.

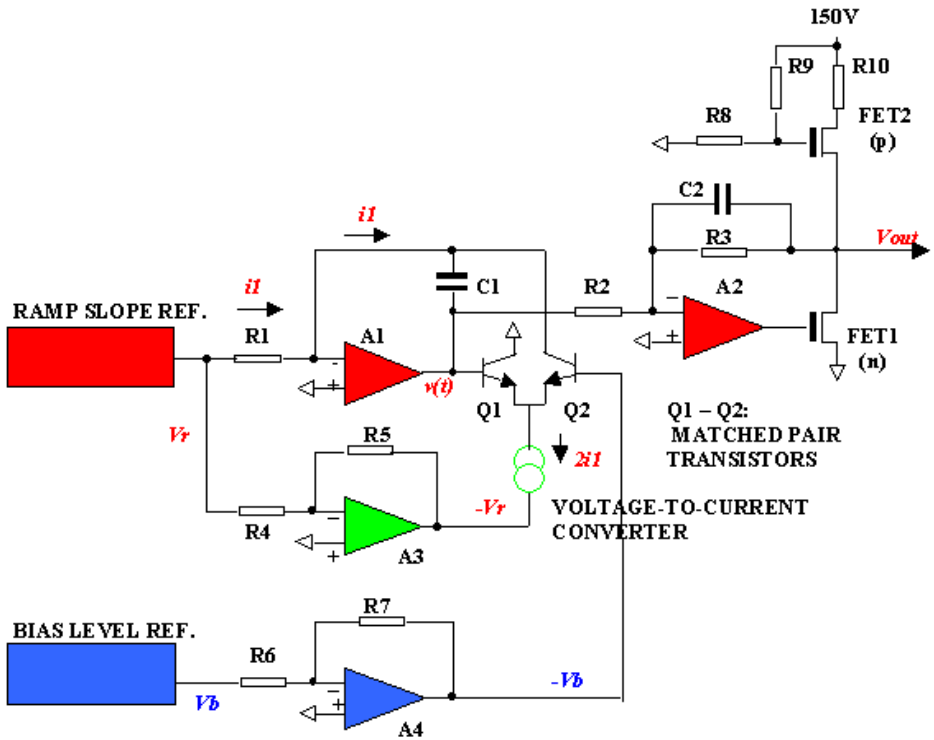
- In the past we erased these effects using a procedure in which the n+ guard is grounded, Vsub is reduced and the parallel clock voltages are increased to invert the charge distribution in the wells. This permits electrons to flow to the interface zone thereby filling the traps.

- We found this approach to work well for small devices but is less satisfactory for large CCDs. Here we examine an alternative approach discovered by our collaborators at Lick Observatory.

New Erasing Technique

- As suggested by Lick we employ the following procedure:
  - Lower V_{sub} to 0 V in a controlled linear manner.
  - Do NOT ground the n+ guard electrode.
  - Increase all the parallel clocks to a voltage high enough to produce inversion and hold them at this value, experimentally found to be 4-5 V above barrier phase.
  - After a brief delay (approx 1 sec.) ramp Vsub back to normal operating voltage (approx. 75 V/s).
  - When V_{sub} > 10 V restore parallel clocks to normal values.
- A special V_{sub} power circuit, designed and constructed by Bojan Turko was used to provide the linear ramp.
- The existing erase function in the VooDoo image acquisition software was modified to provide the additional functionality required.

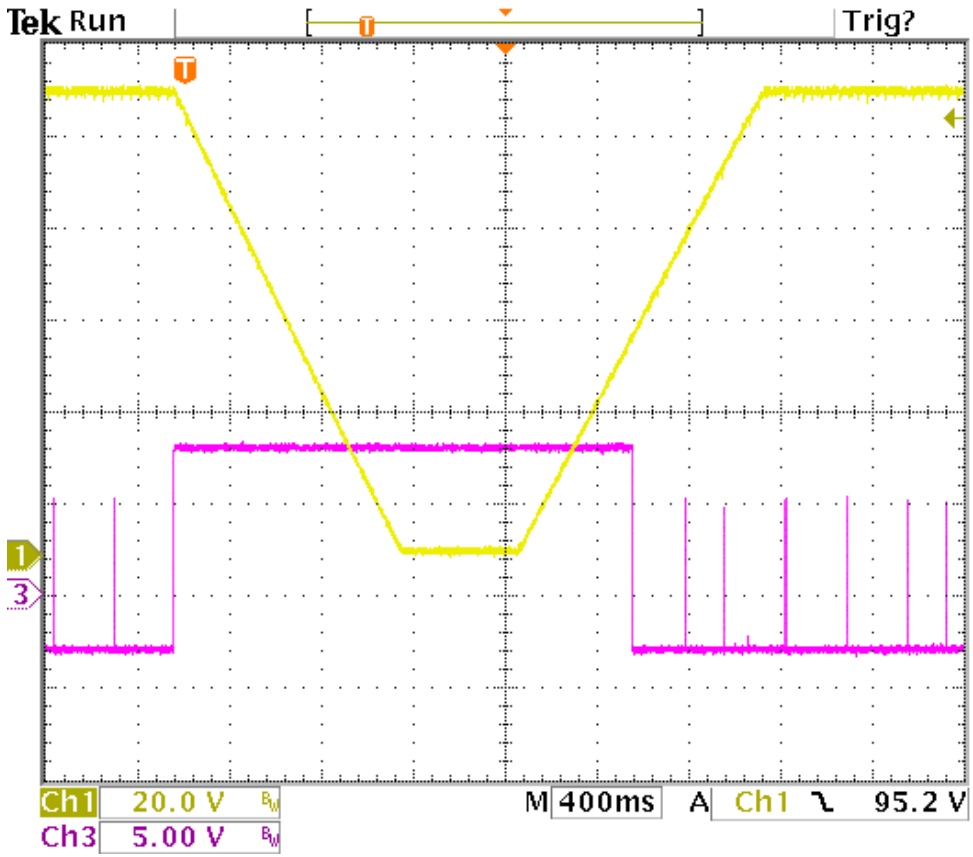
Electronic Control of Substrate Voltage



CCD RESET RAMP GENERATOR BLOCK DIAGRAM

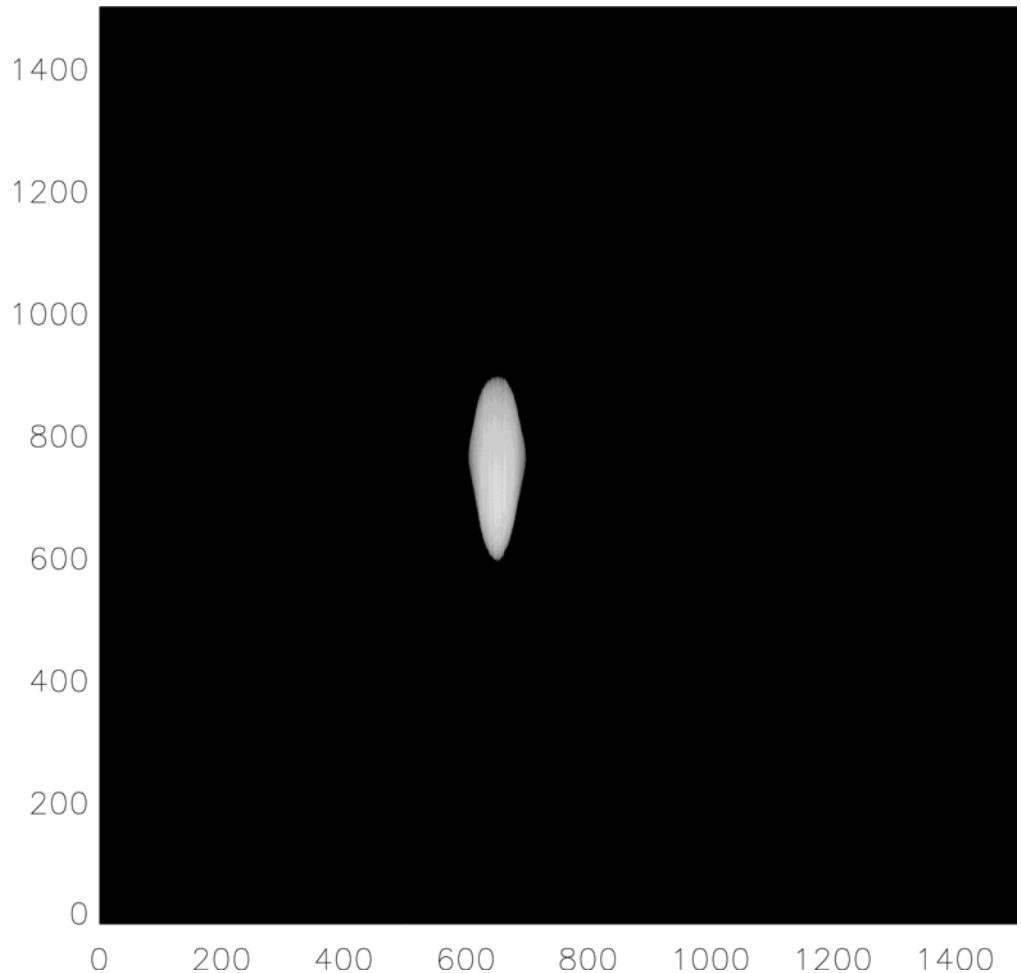
Block diagram showing electronic circuit for ramp control of V_{sub}. Bias level ref. provided by DAC in Leach controller. Slope ref. provided by a second DAC or fixed supply. When the bias level changes, V_{out} is driven at a linear rate by the ramp circuit until balance is achieved in the comparator, Q1-Q2.

Timing of Vsub and Parallel Clocks During Erase



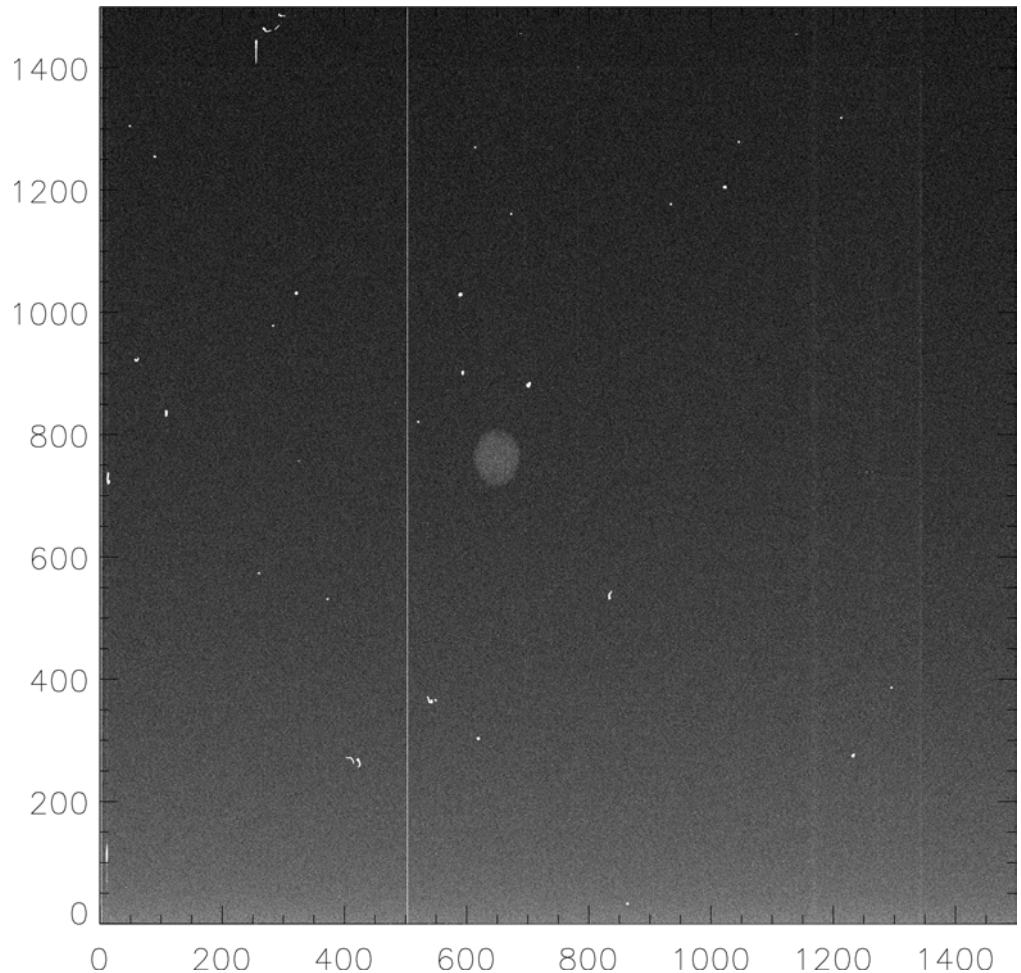
Oscilloscope traces showing (in yellow) timing of Vsub ramp and transition from normal parallel clocking to inversion level (magenta). Key requirements are that Vsub reaches zero while the parallel clocks are in inversion and that it increases to at least ~10V before clocks are restored.

Elimination of Ghost Images by Erase



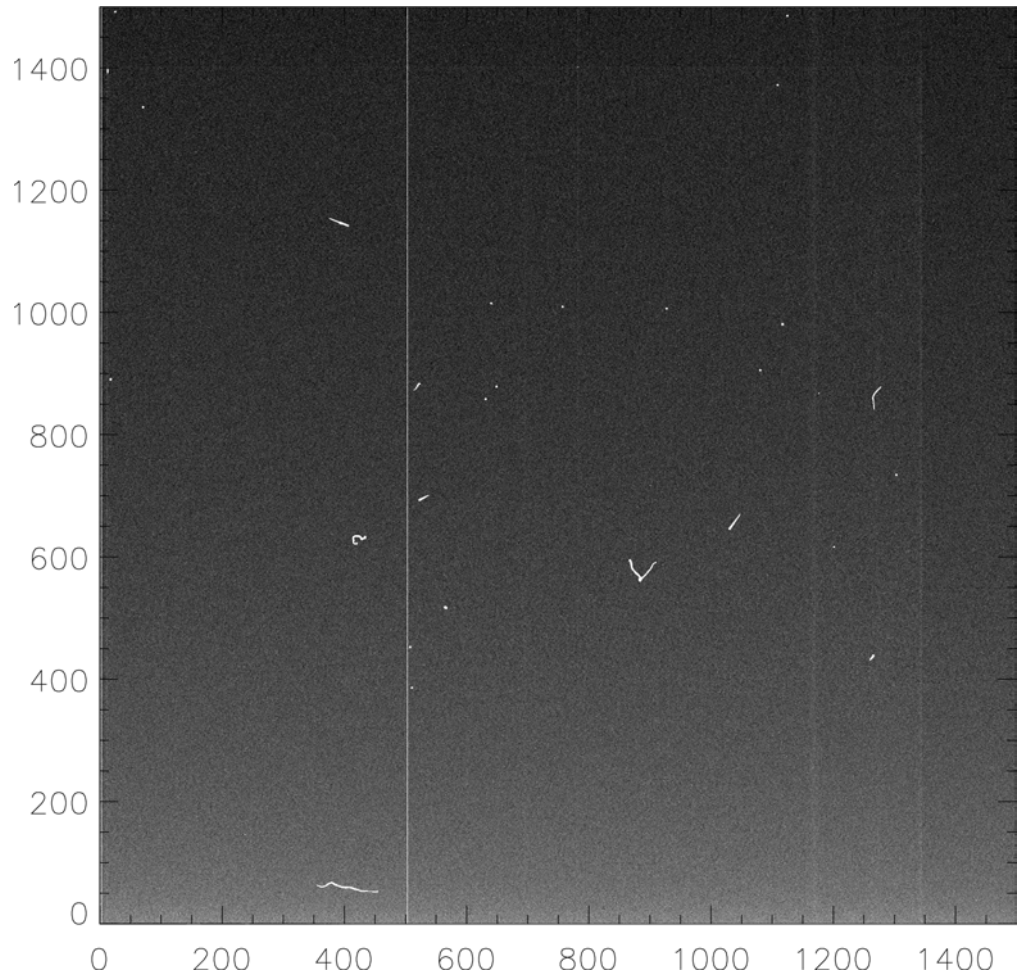
Strong, saturating circular spot image projected onto CCD. Peak intensity approx. 2x full well.

Elimination of Ghost Images by Erase



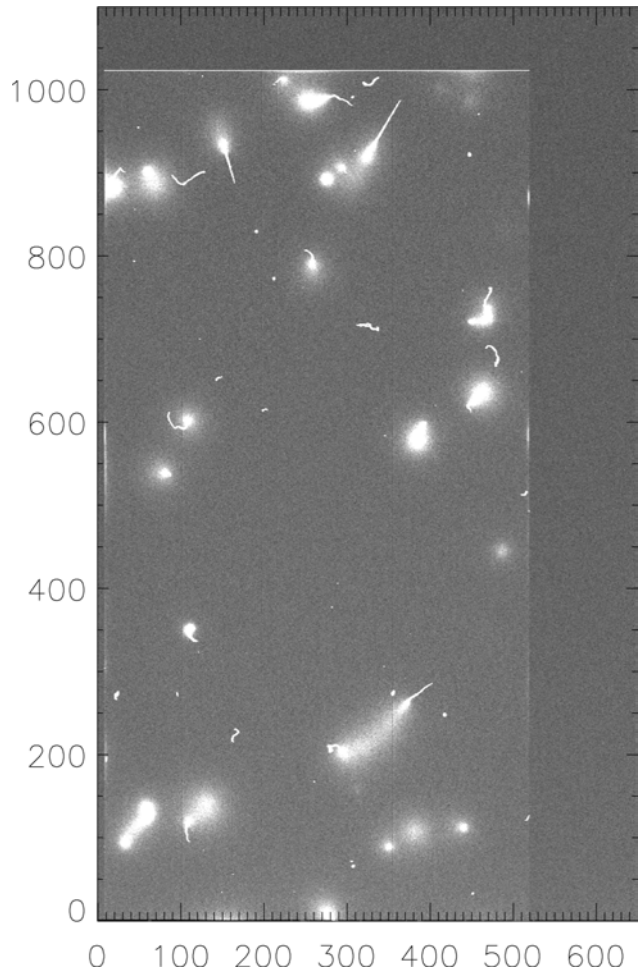
100 second dark image following readout of saturated signal. Weak, but clearly visible (10adu) ghost image is present.

Elimination of Ghost Images by Erase



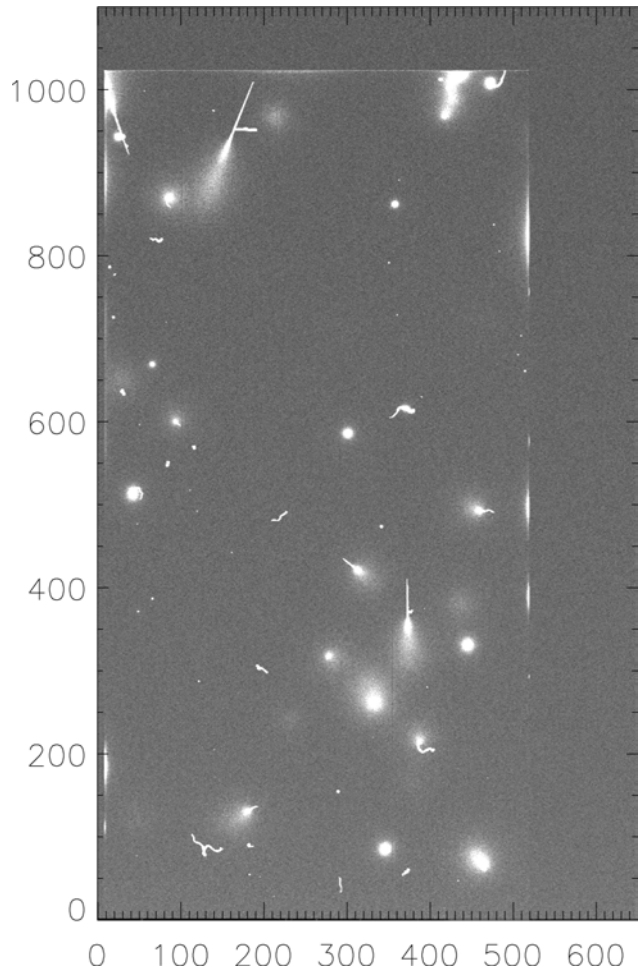
100 second dark image following erase cycle. No residual image can be seen.

Reduction of Dark Current by Erase



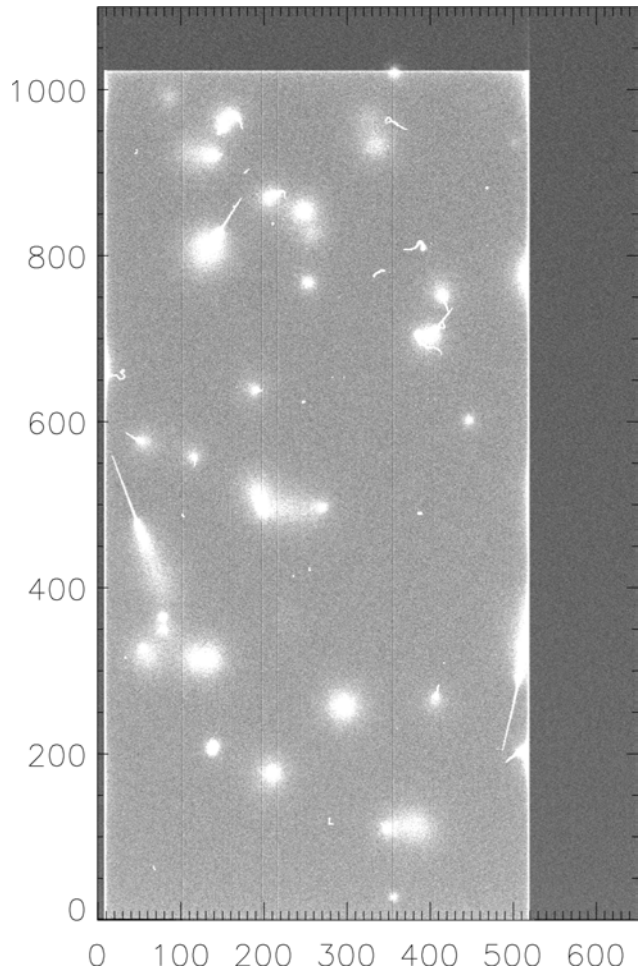
600 sec dark image measured dark current = 26.9 e-/h. Excessive dark current present due to cold turn-on of CCD without erase.

Reduction of Dark Current by Erase



600 sec dark image. Measured dark current = 6.7 e-/hour after erase cycle. Dark current was reduced significantly.

Reduction of Dark Current by Erase



600 sec dark image. Measured dark current = 137 e-/h. Large dark current found when cold cathode vacuum gauge was turned on resulting in light emission. Turn off gauge!!

Conclusions

- Erase technique appears to work well and should be examined further for SNAP application.
- By implementing the erase function directly in the controller DSP code and controlling it through the Voodoo readout software, efficient erasure of persistent images can be obtained.