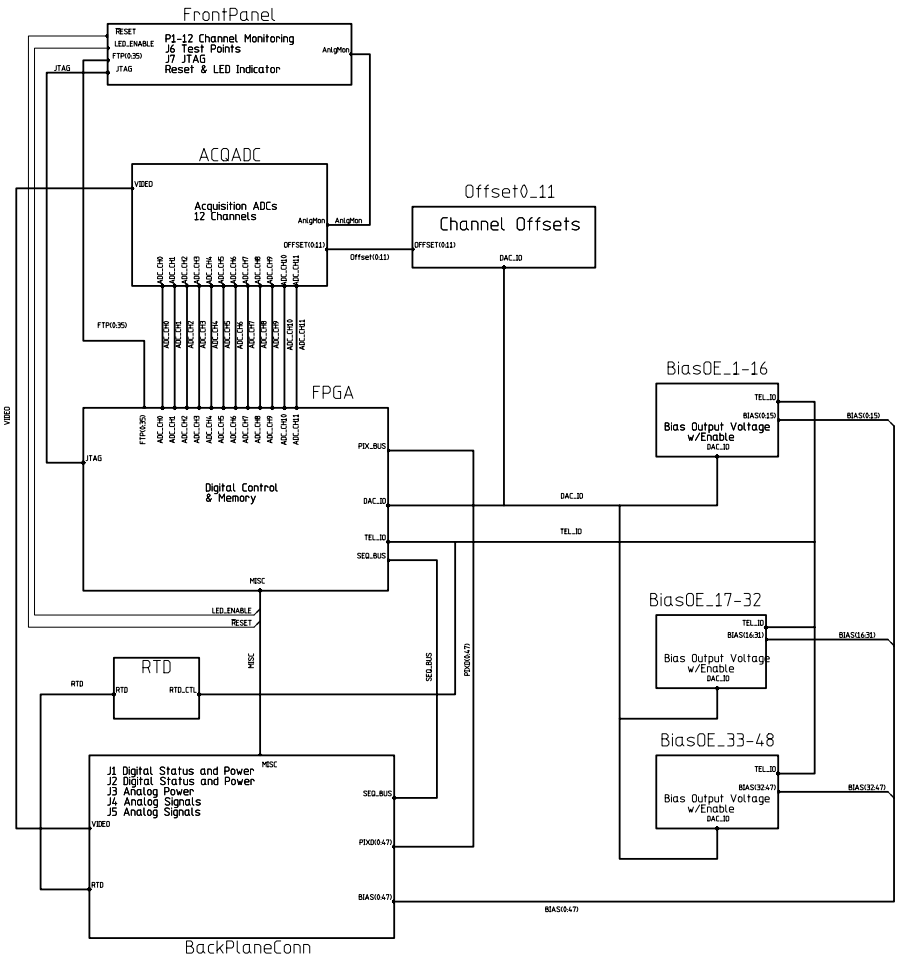


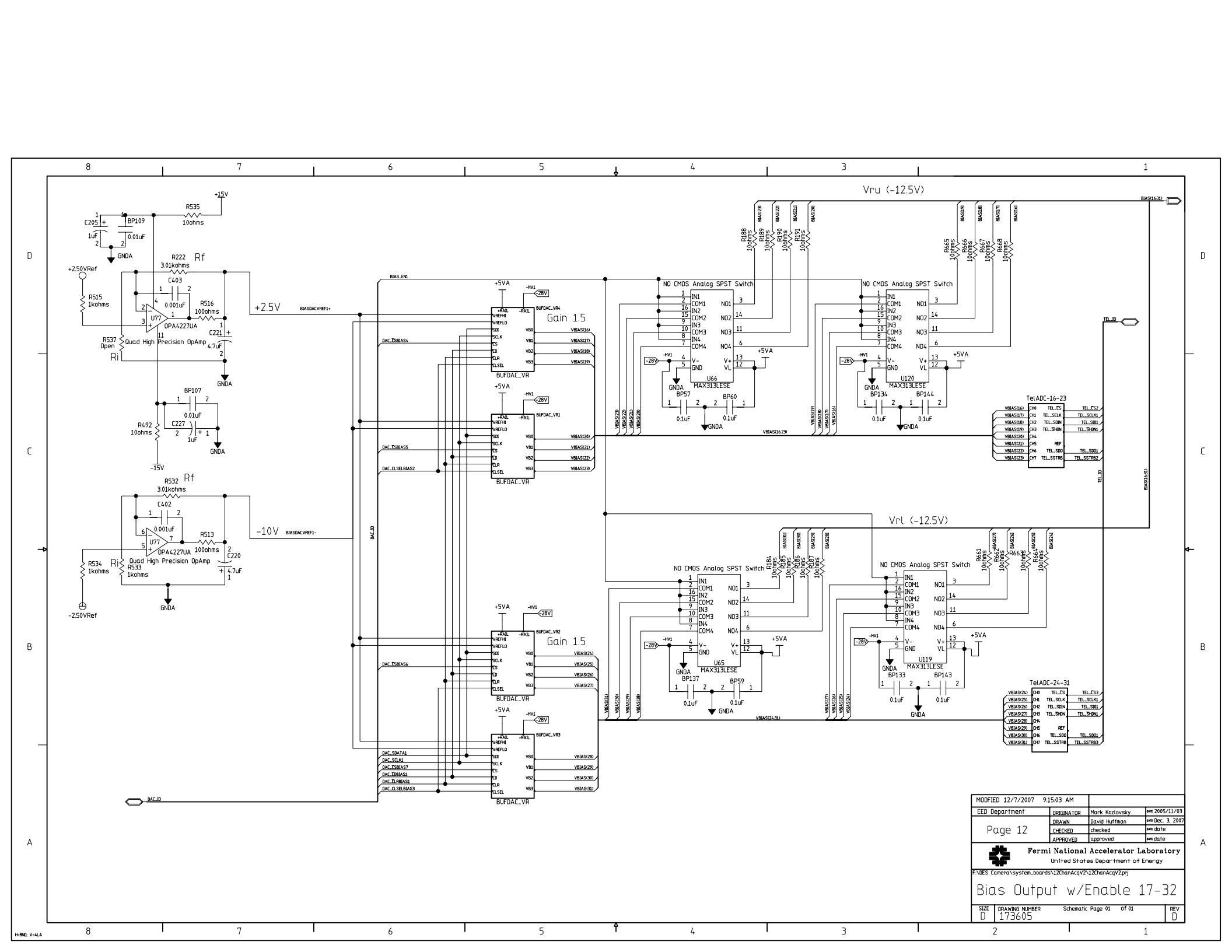
MODIFIED 10/31/2007 11:41:17 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 1	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

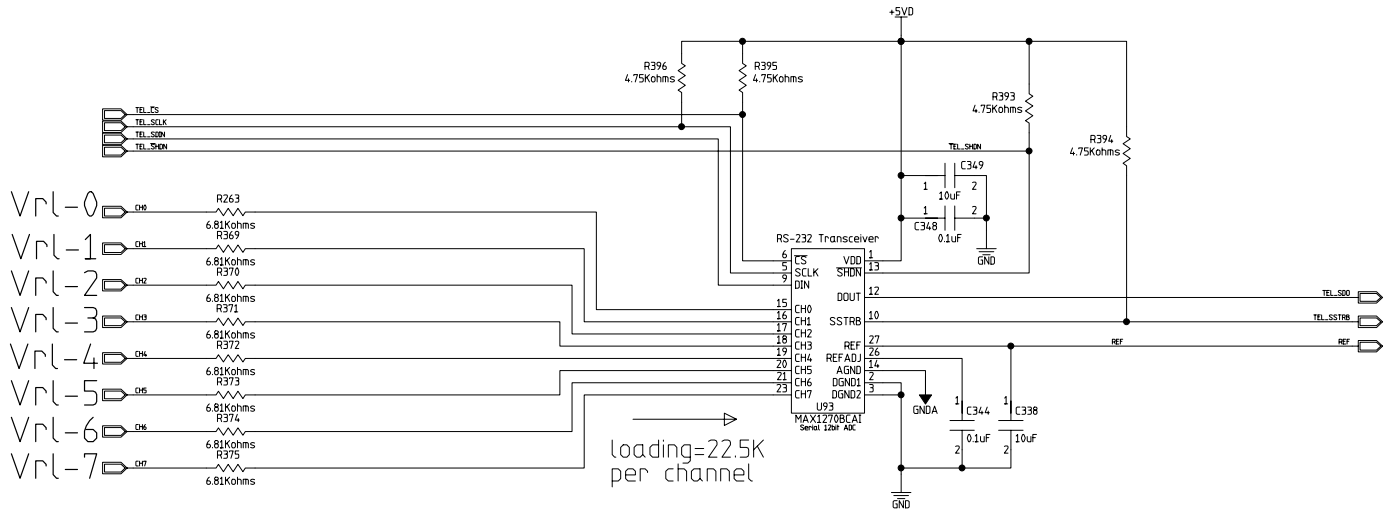
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

ACQUISITION BOARD TOP LEVEL

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D


Vru (-12.5V)
Vrl (-12.5V)
+2.5V
-10V
+2.50VRef
-2.50VRef
Gain 1.5
Gain 1.5
NO CMOS Analog SPST Switch
NO CMOS Analog SPST Switch
NO CMOS Analog SPST Switch
NO CMOS Analog SPST Switch
Quad High Precision OpAmp
Quad High Precision OpAmp
OPA4227UA
MAX313LESE
BUFDAC_VR
BUFDAC_VR1
BUFDAC_VR2
BUFDAC_VR3
BUFDAC_VR4
TelADC-16-23
TelADC-24-31
Fermi National Accelerator Laboratory
United States Department of Energy
Bias Output w/Enable 17-32
MODIFIED 12/7/2007 9:15:03 AM
EED Department
Page 12
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



TELEMETRY CHANNELS BIAS 24-31
READ Memory Location 0x458-45F

MODFIED 12/7/2007 9:03:51 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

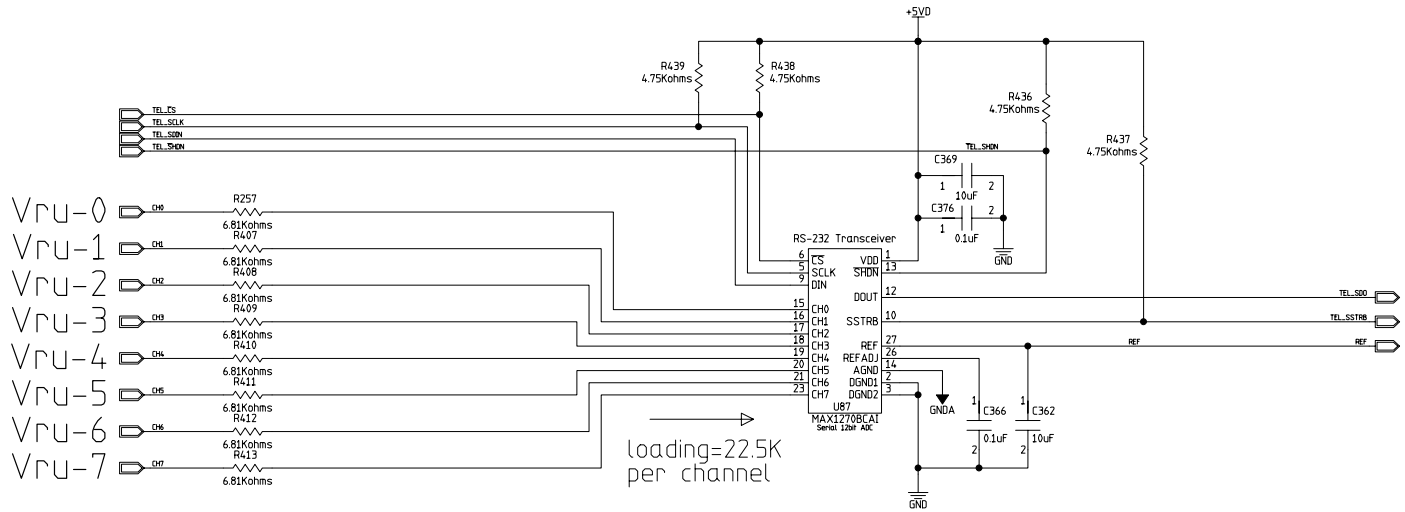
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Telemetry ADC 24-31

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 16-23
READ Memory Location 0x450-457

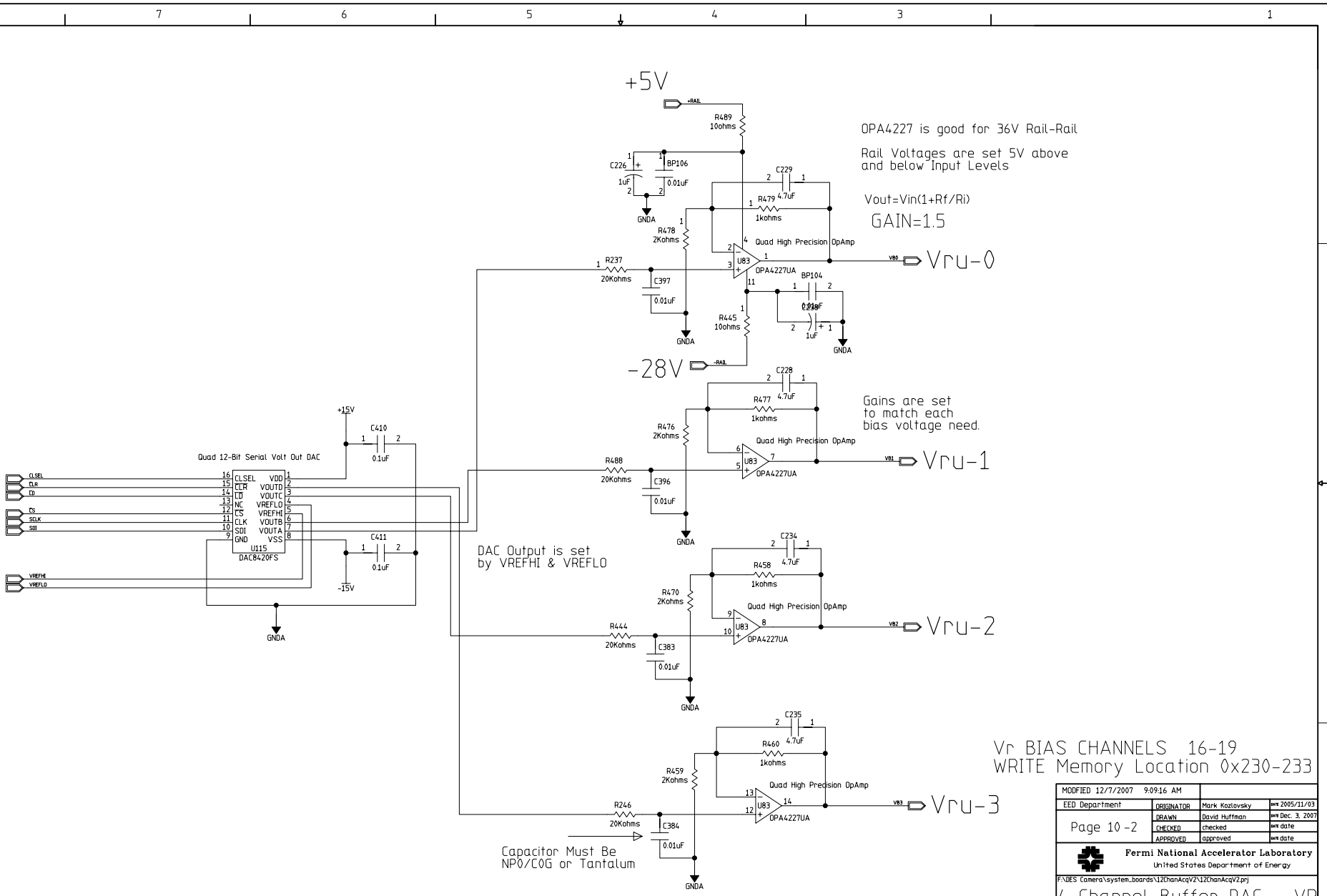
MODFIED 12/7/2007 9:03:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

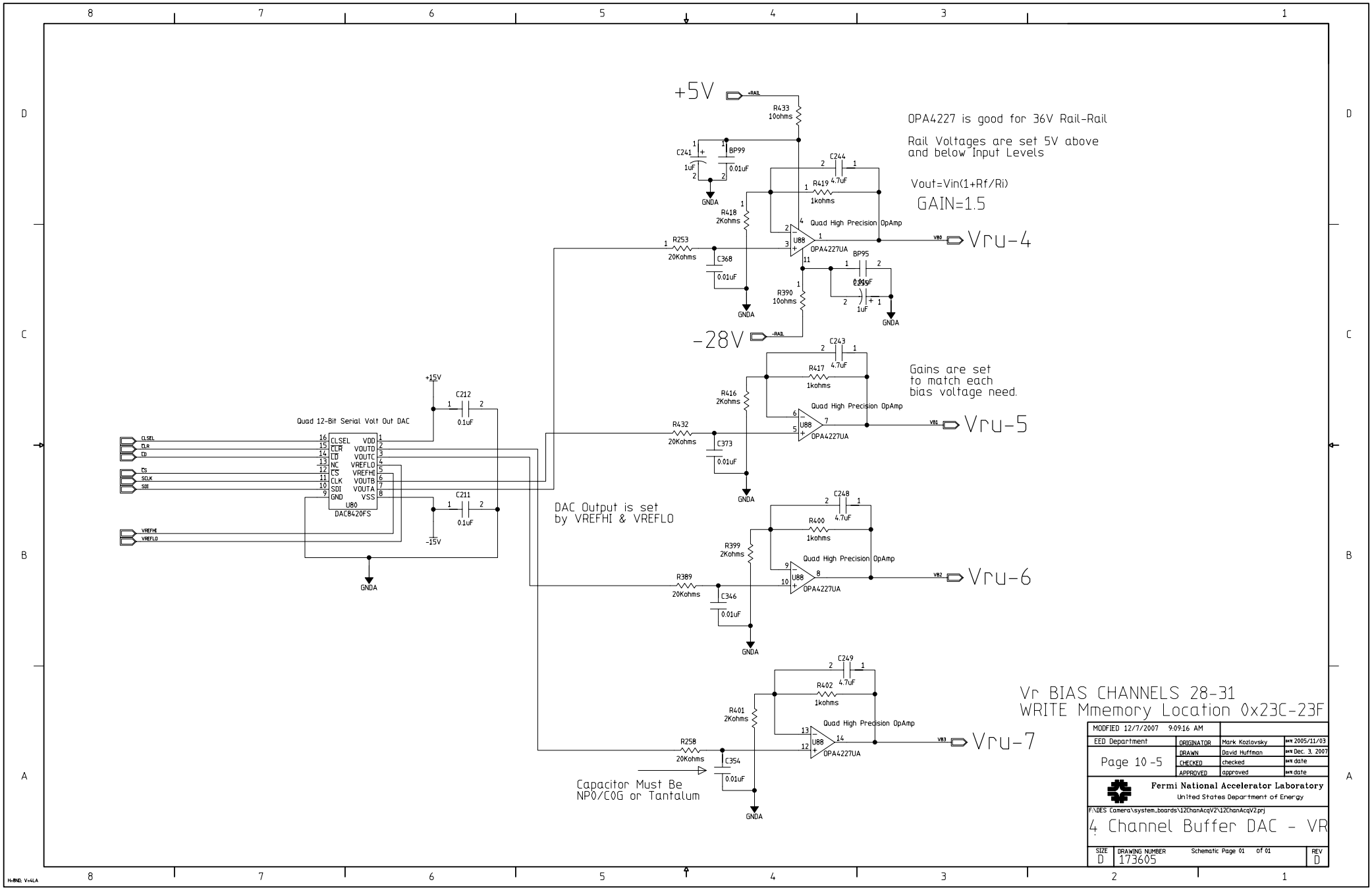
Fermi National Accelerator Laboratory
United States Department of Energy

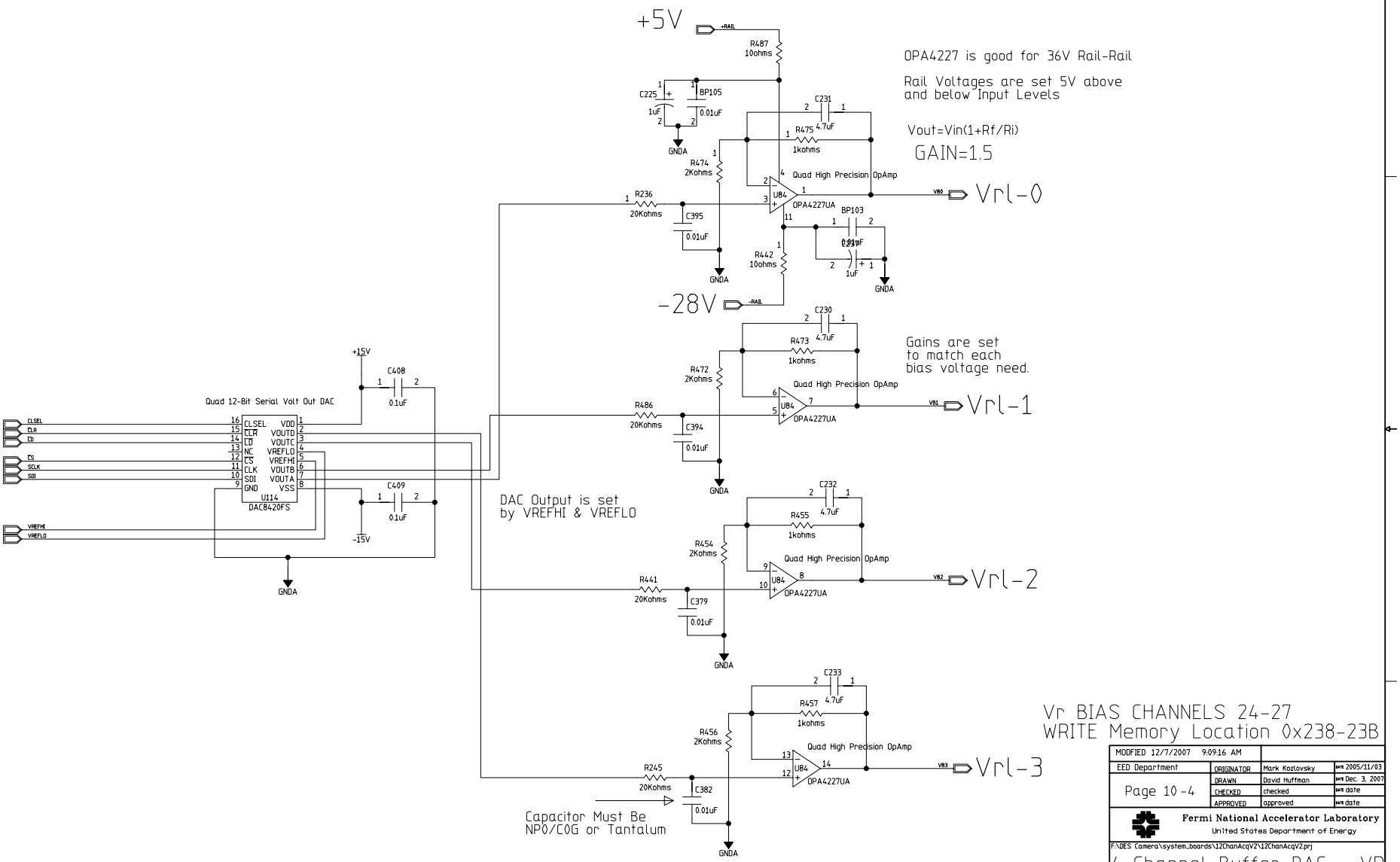
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

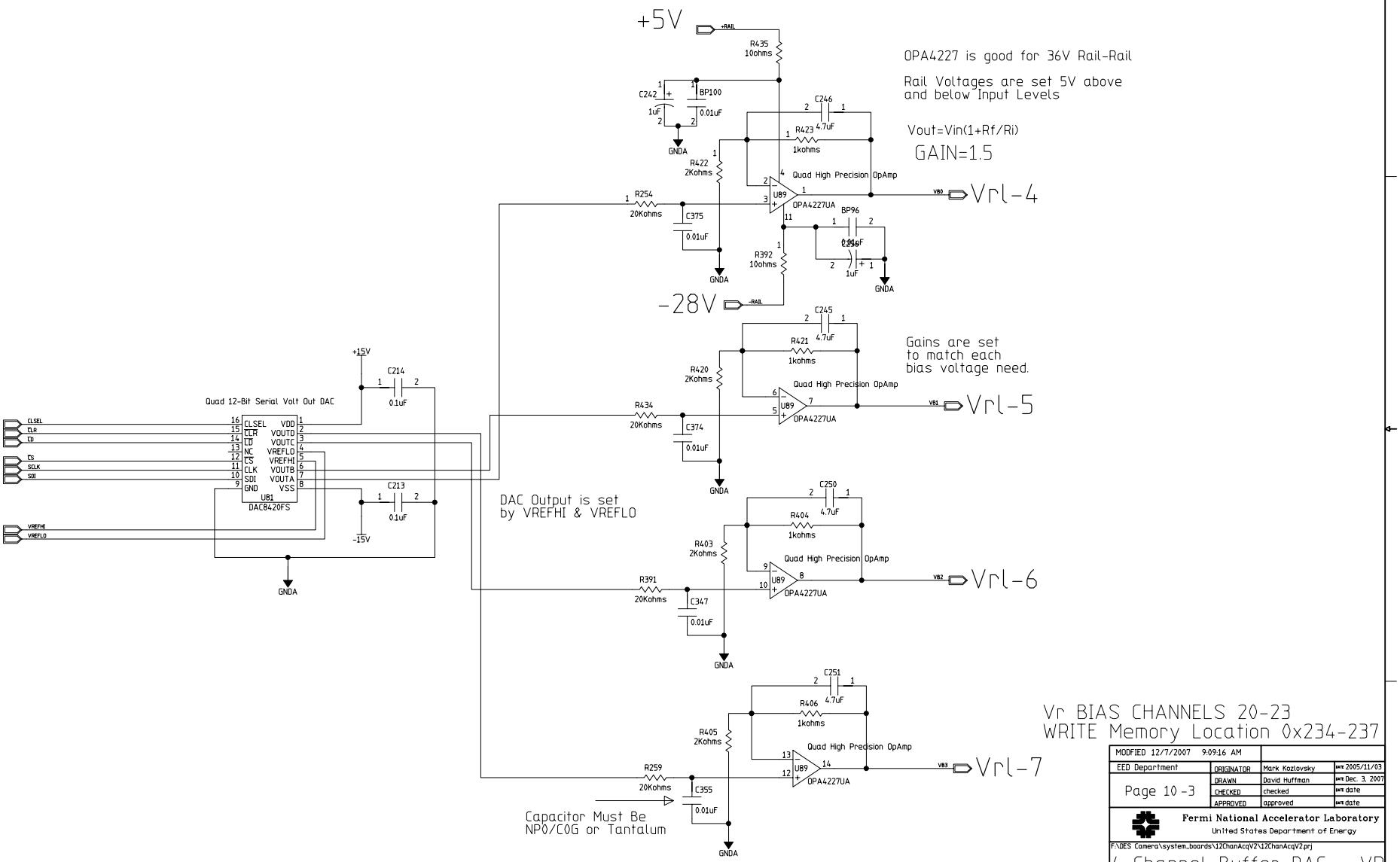
Telemetry ADC 16-23

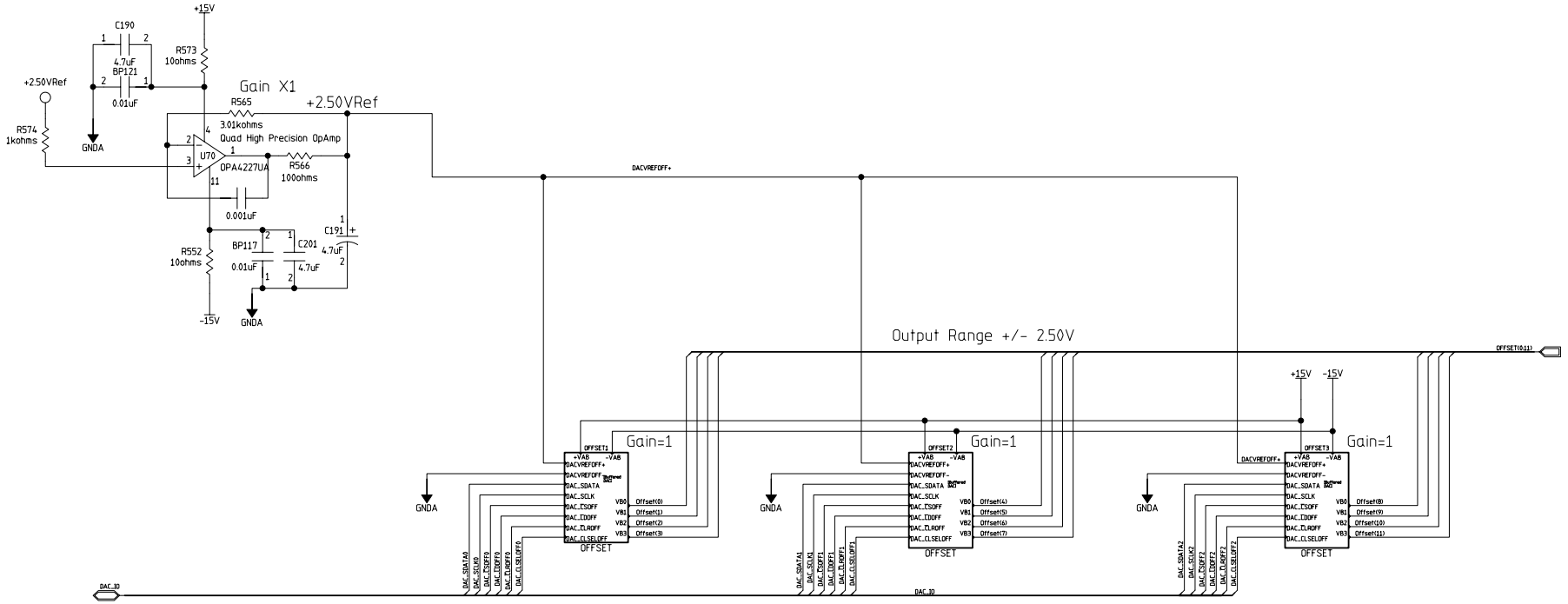
SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D


+5V
-28V
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
Gains are set
to match each
bias voltage need.
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
U115
Quad High Precision OpAmp
OPA4227UA
U83
Vru-0
Vru-1
Vru-2
Vru-3
DAC Output is set
by VREFHI & VREFLO
Capacitor Must Be
NP0/C0G or Tantalum
GNDA
+15V
-15V
Vr BIAS CHANNELS 16-19
WRITE Memory Location 0x230-233
Fermi National Accelerator Laboratory
United States Department of Energy
4 Channel Buffer DAC - VR
Page 10 -2
DRAWING NUMBER 173605
Schematic Page 01 of 01
SIZE D
REV D


+5V
+RAIL
R433
10ohms
C241
1uF
BP99
0.01uF
GNDA
C244
4.7uF
R419
1kohms
R418
2Kohms
Quad High Precision OpAmp
U88
OPA4227UA
R253
20Kohms
C368
0.01uF
BP95
0.01uF
1uF
R390
10ohms
-28V
-RAIL
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
VB0
Vru-4
C243
4.7uF
R417
1kohms
R416
2Kohms
R432
20Kohms
C373
0.01uF
Gains are set
to match each
bias voltage need.
VB1
Vru-5
C248
4.7uF
R400
1kohms
R399
2Kohms
R389
20Kohms
C346
0.01uF
VB2
Vru-6
C249
4.7uF
R402
1kohms
R401
2Kohms
R258
20Kohms
C354
0.01uF
VB3
Vru-7
+15V
C212
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U80
DAC8420FS
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
C211
0.1uF
-15V
DAC Output is set
by VREFHI & VREFLO
Capacitor Must Be
NP0/C0G or Tantalum
Vr BIAS CHANNELS 28-31
WRITE Mmemory Location 0x23C-23F
MODFIED 12/7/2007 9:09:16 AM
EED Department
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Page 10-5
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


+5V
+RAIL
R487
10ohms
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
C225
1uF
BP105
0.01uF
C231
4.7uF
R475
1kohms
R474
2Kohms
Quad High Precision OpAmp
U84
OPA4227UA
VB0
Vrl-0
R236
20Kohms
C395
0.01uF
BP103
0.01uF
R442
10ohms
1uF
GNDA
-28V
-RAIL
C230
4.7uF
R473
1kohms
R472
2Kohms
Gains are set
to match each
bias voltage need.
Quad High Precision OpAmp
U84
OPA4227UA
VB1
Vrl-1
R486
20Kohms
C394
0.01uF
+15V
C408
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U114
DAC8420FS
CLSEL
CLR
LD
NC
CS
CLK
SDI
GND
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
C409
0.1uF
-15V
GNDA
DAC Output is set
by VREFHI & VREFLO
C232
4.7uF
R455
1kohms
R454
2Kohms
Quad High Precision OpAmp
U84
OPA4227UA
VB2
Vrl-2
R441
20Kohms
C379
0.01uF
C233
4.7uF
R457
1kohms
R456
2Kohms
Quad High Precision OpAmp
U84
OPA4227UA
VB3
Vrl-3
R245
20Kohms
C382
0.01uF
Capacitor Must Be
NP0/C0G or Tantalum
Vr BIAS CHANNELS 24-27
WRITE Memory Location 0x238-23B
MODIFIED 12/7/2007 9:09:16 AM
EED Department
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Page 10-4
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


+5V
+RAIL
R435
10ohms
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
C242
1uF
BP100
0.01uF
GNDA
C246
4.7uF
R423
1kohms
R422
2Kohms
Quad High Precision OpAmp
U89
OPA4227UA
VB0
Vrl-4
R254
20Kohms
C375
0.01uF
BP96
0.01uF
C340
1uF
R392
10ohms
-28V
-RAIL
C245
4.7uF
R421
1kohms
R420
2Kohms
Gains are set
to match each
bias voltage need.
Quad High Precision OpAmp
U89
OPA4227UA
VB1
Vrl-5
R434
20Kohms
C374
0.01uF
GNDA
C250
4.7uF
R404
1kohms
R403
2Kohms
Quad High Precision OpAmp
U89
OPA4227UA
VB2
Vrl-6
R391
20Kohms
C347
0.01uF
GNDA
C251
4.7uF
R406
1kohms
R405
2Kohms
Quad High Precision OpAmp
U89
OPA4227UA
VB3
Vrl-7
R259
20Kohms
C355
0.01uF
GNDA
Capacitor Must Be
NP0/C0G or Tantalum
+15V
C214
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U81
DAC8420FS
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
C213
0.1uF
-15V
GNDA
DAC Output is set
by VREFHI & VREFLO
Vr BIAS CHANNELS 20-23
WRITE Memory Location 0x234-237
MODIFIED 12/7/2007 9:09:16 AM
EED Department
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Page 10-3
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



ADC Offset CHANNELS 0-11
WRITE Memory Location 0x210-21B

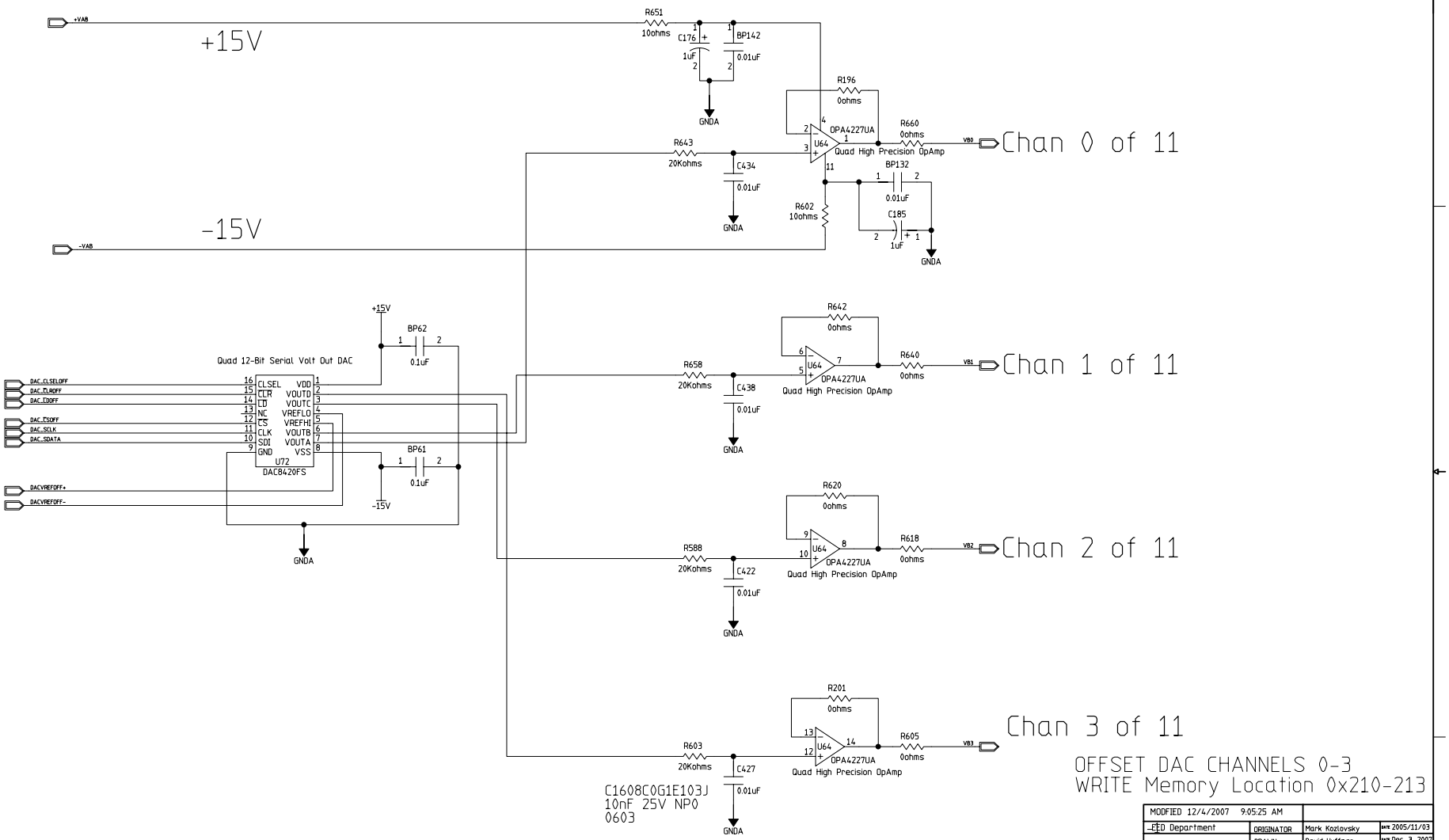
MODFIED 12/4/2007 9:23:06 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 15	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

OFFSET VOLTAGE 0-11

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D



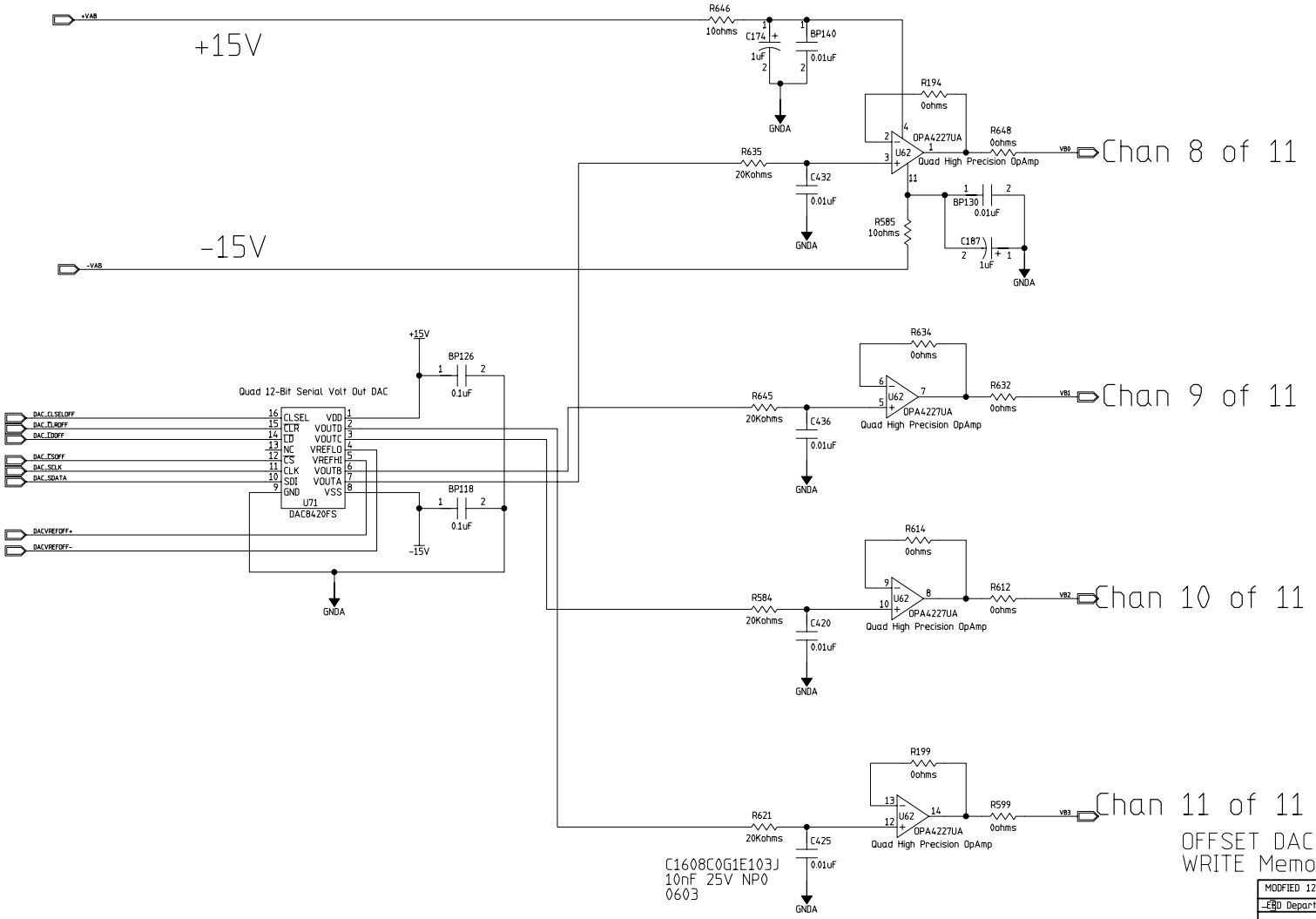
MODIFIED 12/4/2007 9:05:25 AM			
-ED Department	ORIGINATOR	Mark Kozlovsky	date 2005/11/03
Page 16	DRAWN	David Huffman	date Dec. 3, 2007
	CHECKED	checked	date date
	APPROVED	approved	date date

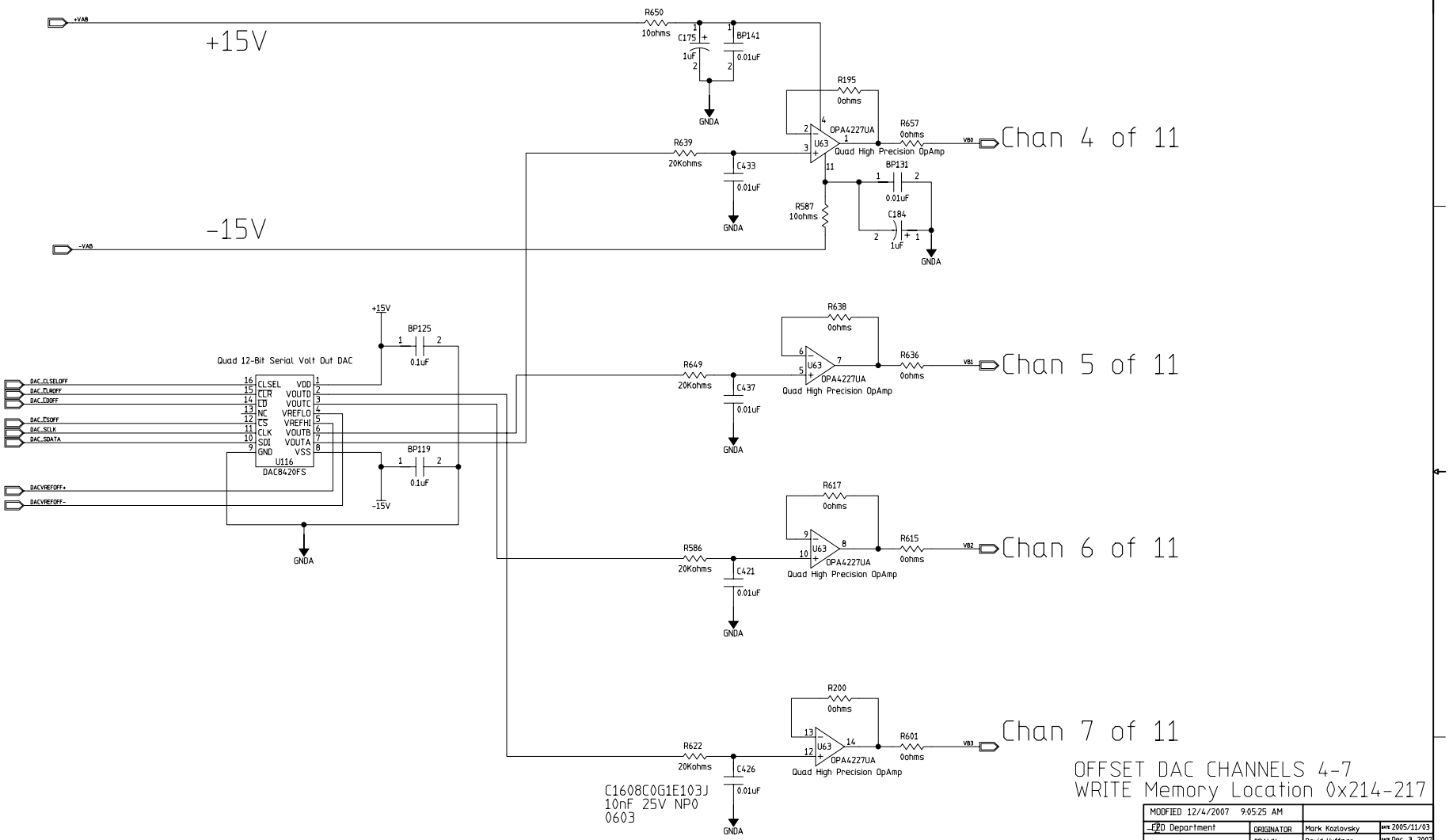
Fermi National Accelerator Laboratory
United States Department of Energy

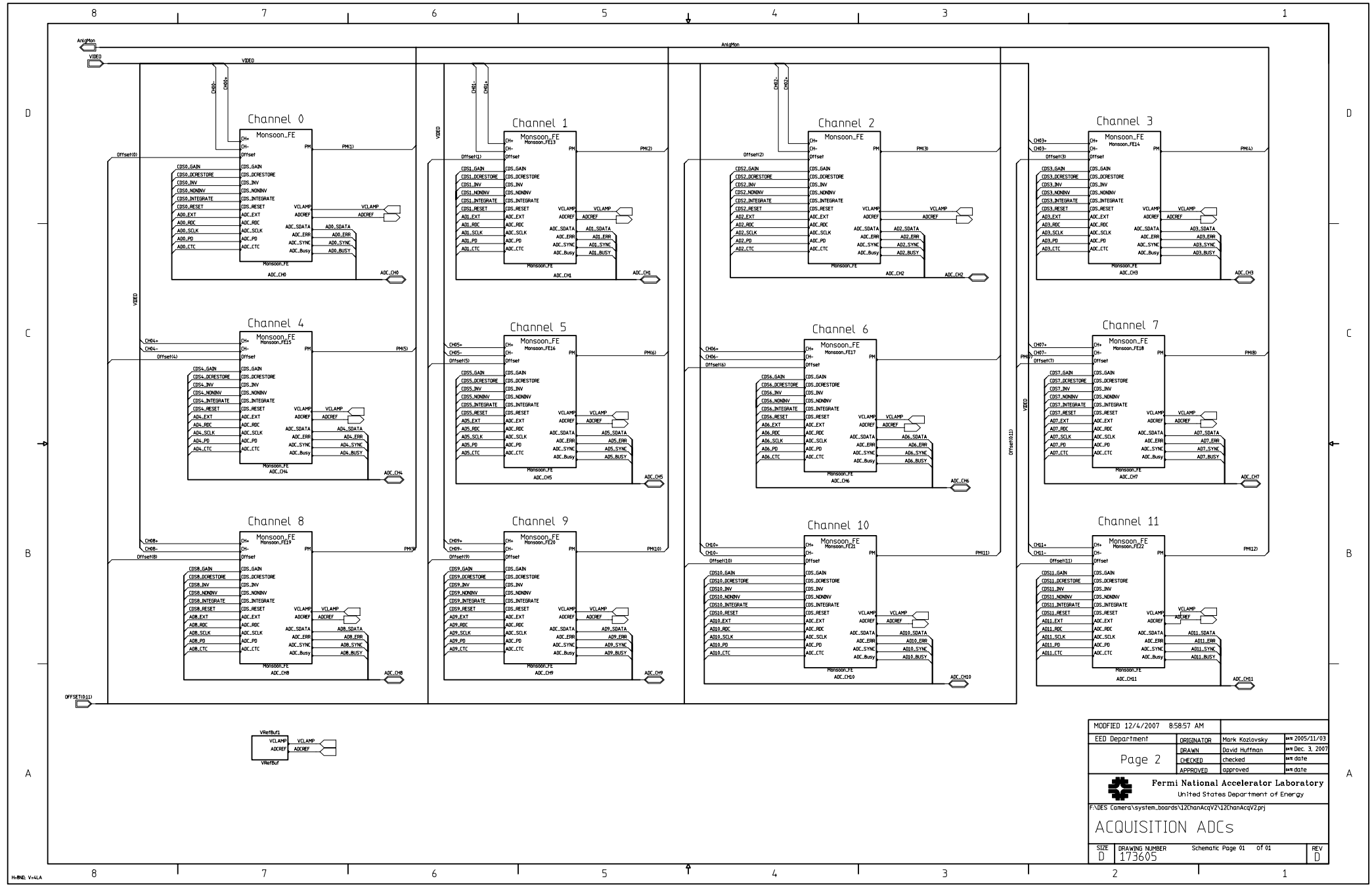
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

OFFSET DAC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D


+15V
-15V
+VAB
-VAB
R646
10ohms
C174
1uF
BP140
0.01uF
GNDA
R194
0ohms
OPA4227UA
U62
Quad High Precision OpAmp
R648
0ohms
VB0
Chan 8 of 11
R635
20Kohms
C432
0.01uF
R585
10ohms
BP130
0.01uF
C187
1uF
Quad 12-Bit Serial Volt Out DAC
DAC_CLSELOFF
DAC_CLROFF
DAC_CDOFF
DAC_CSOFF
DAC_SCLK
DAC_SDATA
CLSEL
CLR
LD
NC
CS
CLK
SDI
GND
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
U71
DAC8420FS
BP126
BP118
0.1uF
DACVREFOFF+
DACVREFOFF-
R634
0ohms
R645
20Kohms
C436
0.01uF
R632
0ohms
VB1
Chan 9 of 11
R614
0ohms
R584
20Kohms
C420
0.01uF
R612
0ohms
VB2
Chan 10 of 11
R199
0ohms
R621
20Kohms
C425
0.01uF
R599
0ohms
VB3
Chan 11 of 11
C1608C0G1E103J
10nF 25V NP0
0603
OFFSET DAC CHANNELS 8-11
WRITE Memory Location 0x218-21B
MODIFIED 12/4/2007 9:05:25 AM
-ERD Department
Page 16
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
OFFSET DAC
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


+VAB
+15V
R650
10ohms
C175
1uF
BP141
0.01uF
GNDA
R195
0ohms
OPA4227UA
U63
Quad High Precision OpAmp
R657
0ohms
VB0
Chan 4 of 11
R639
20Kohms
C433
0.01uF
BP131
0.01uF
R587
10ohms
C184
1uF
-VAB
-15V
+15V
BP125
0.1uF
Quad 12-Bit Serial Volt Out DAC
DAC_CLSELOFF
DAC_CLROFF
DAC_LDOFF
DAC_CSOFF
DAC_SCLK
DAC_SDATA
CLSEL
CLR
LD
NC
CS
CLK
SDI
GND
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
U116
DAC8420FS
BP119
0.1uF
-15V
DACVREFOFF+
DACVREFOFF-
GNDA
R638
0ohms
R649
20Kohms
C437
0.01uF
R636
0ohms
VB1
Chan 5 of 11
R617
0ohms
R586
20Kohms
C421
0.01uF
R615
0ohms
VB2
Chan 6 of 11
R200
0ohms
R622
20Kohms
C426
0.01uF
R601
0ohms
VB3
Chan 7 of 11
C1608C0G1E103J
10nF 25V NP0
0603
OFFSET DAC CHANNELS 4-7
WRITE Memory Location 0x214-217
MODIFIED 12/4/2007 9:05:25 AM
ED Department
Page 16
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
OFFSET DAC
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



MODIFIED 12/4/2007 8:58:57 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 2	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

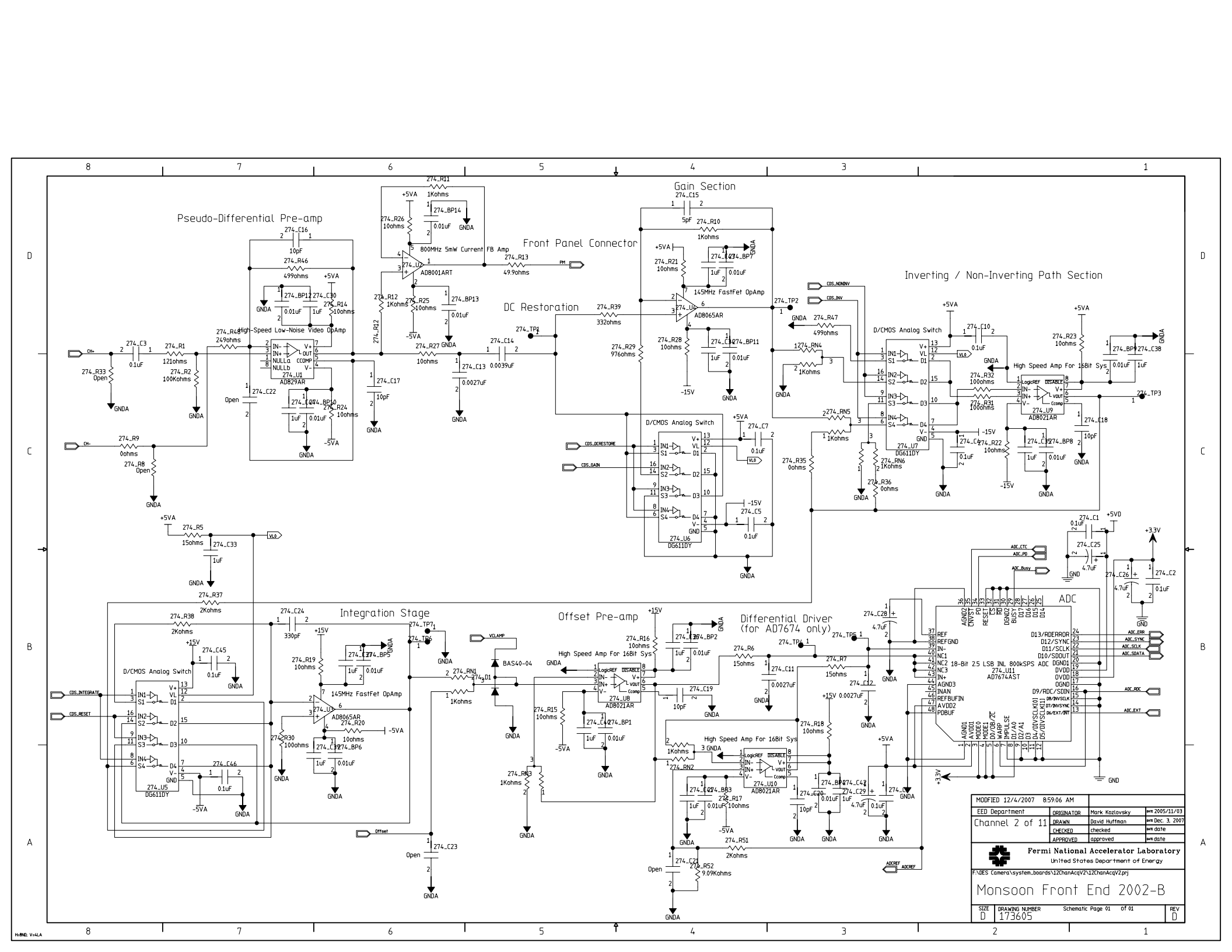
Fermi National Accelerator Laboratory
United States Department of Energy

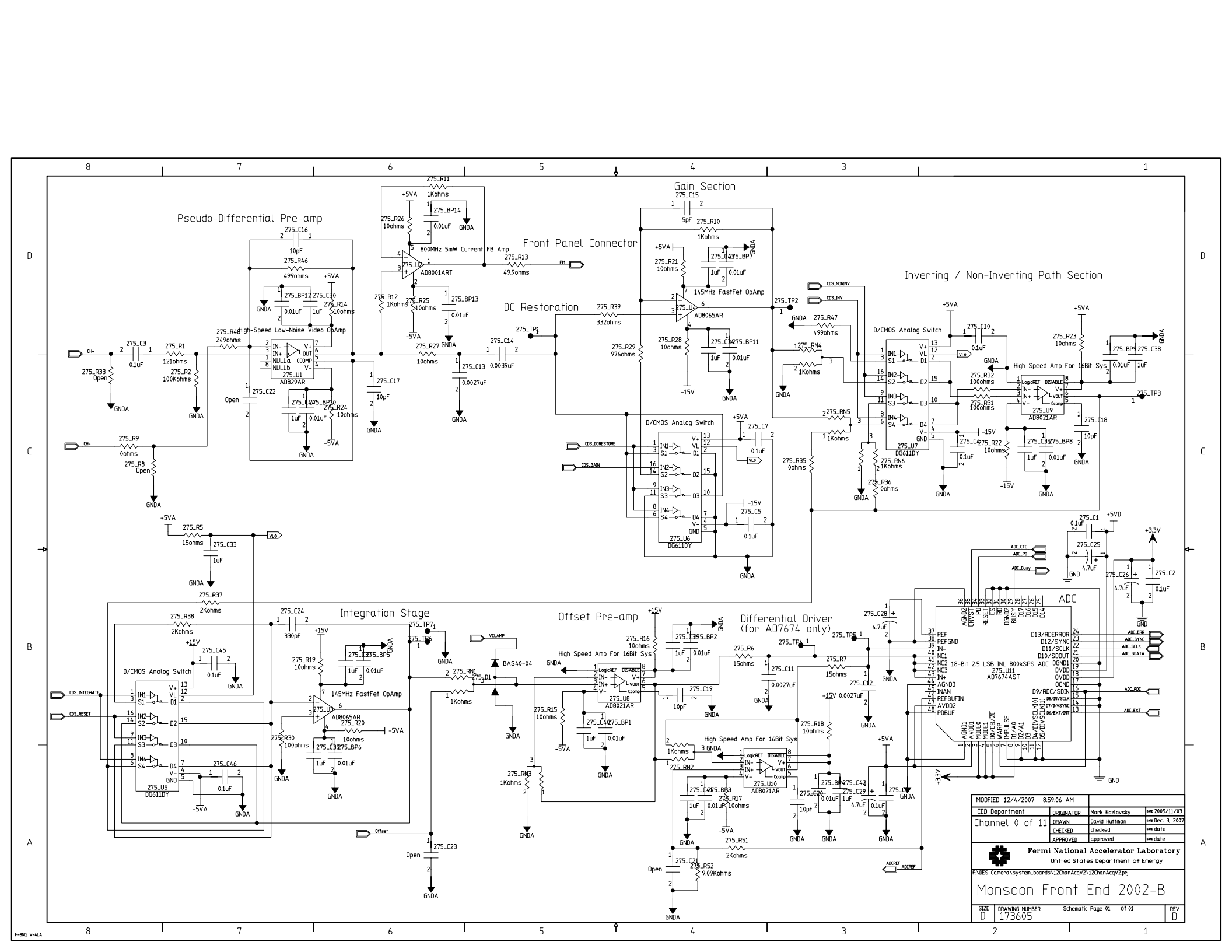
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

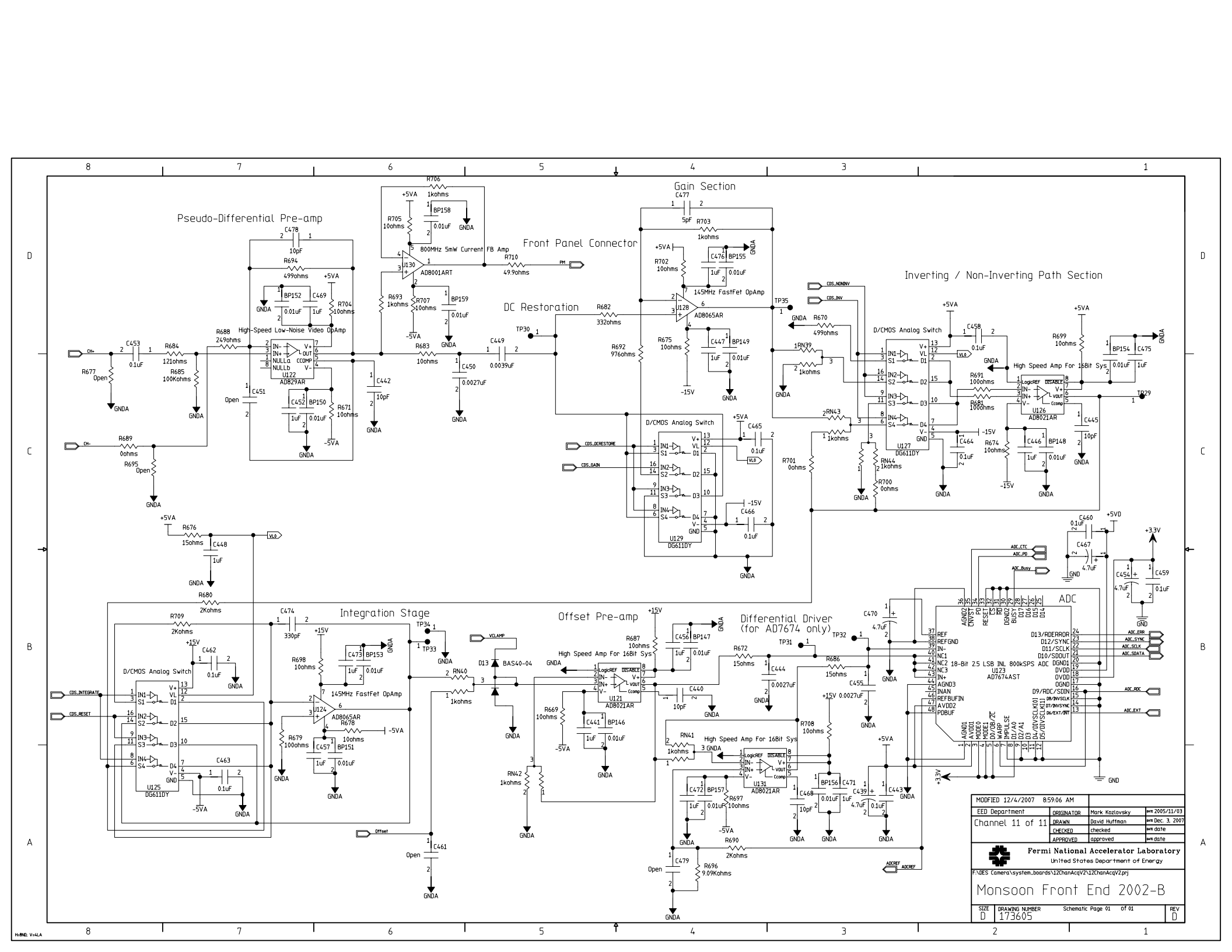
ACQUISITION ADCs

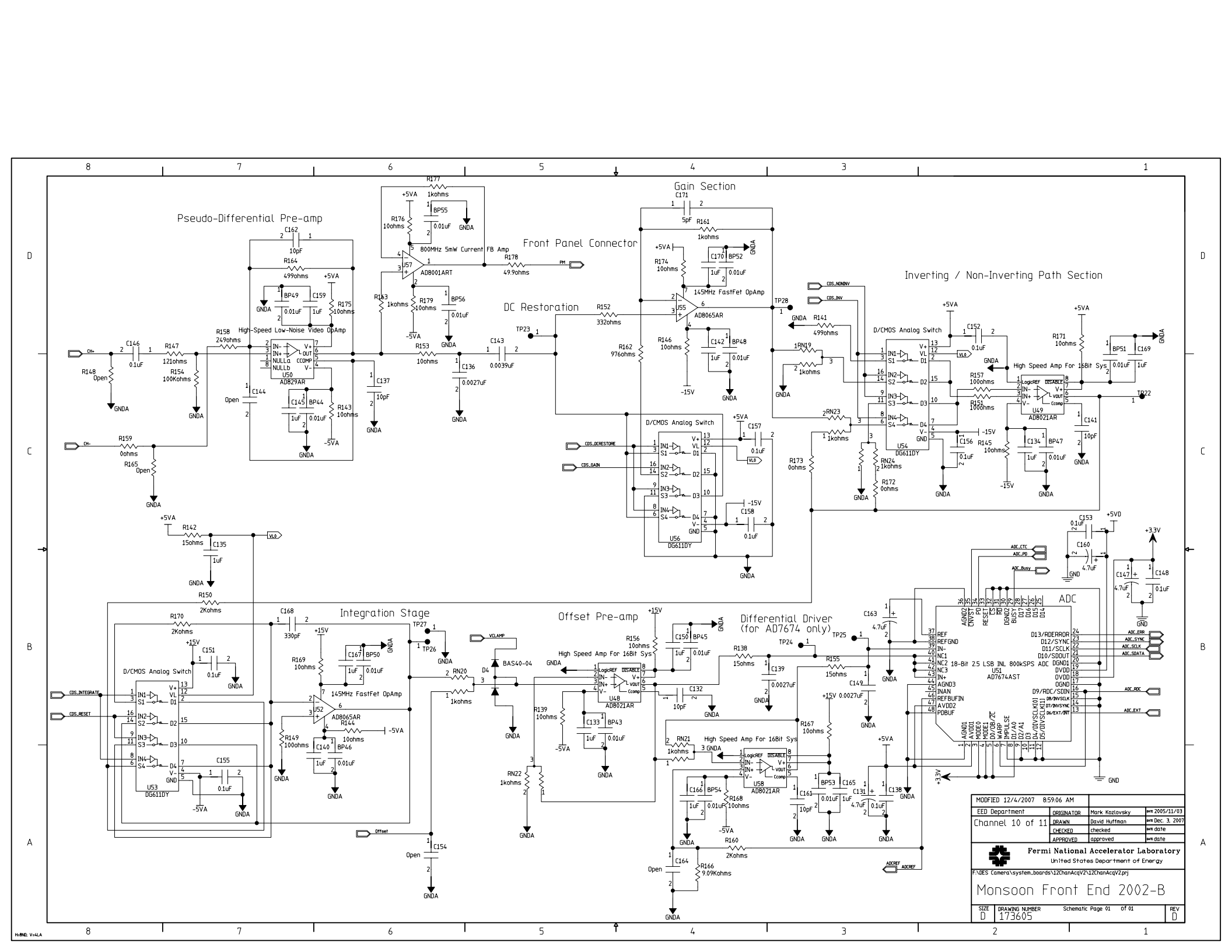
SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

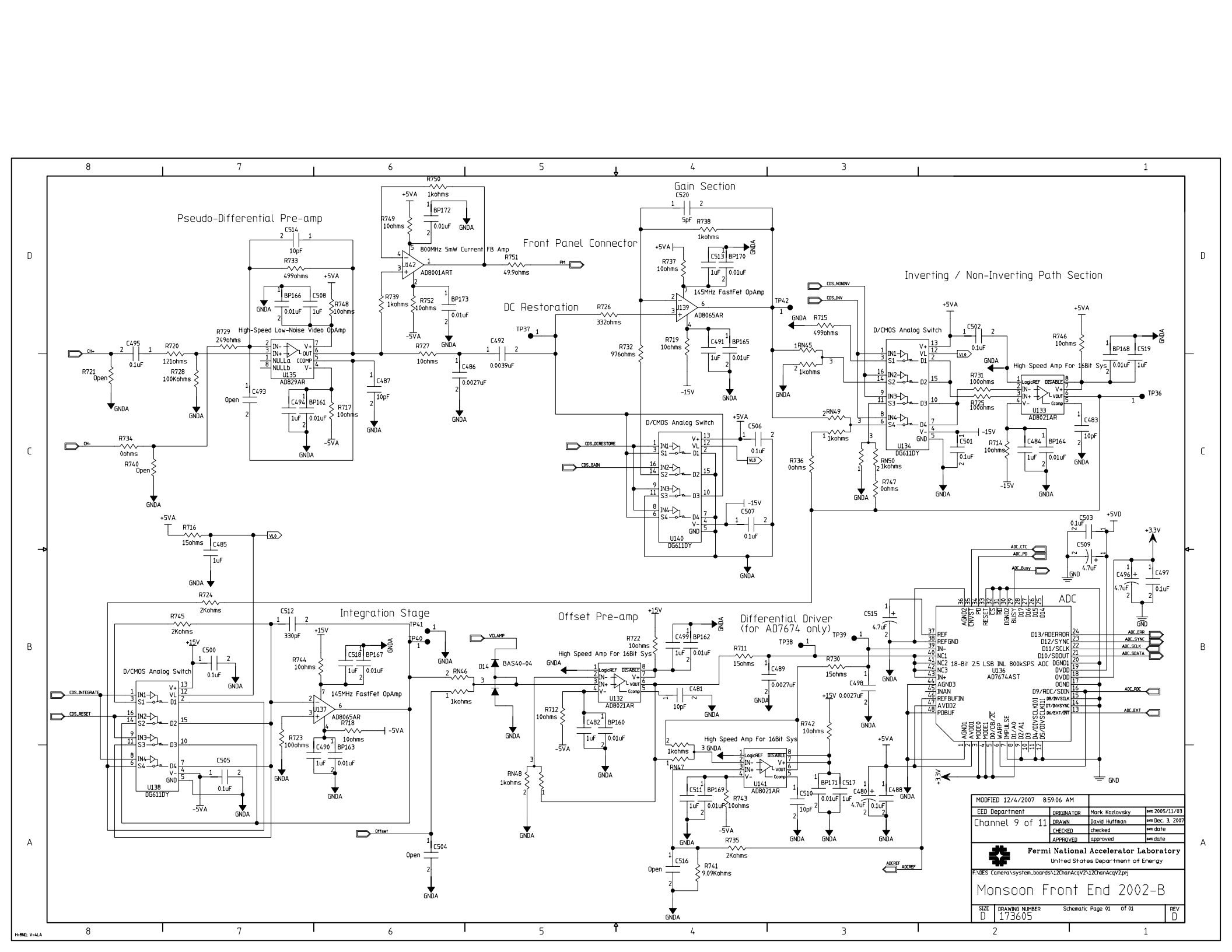
H-BND: V=4LA

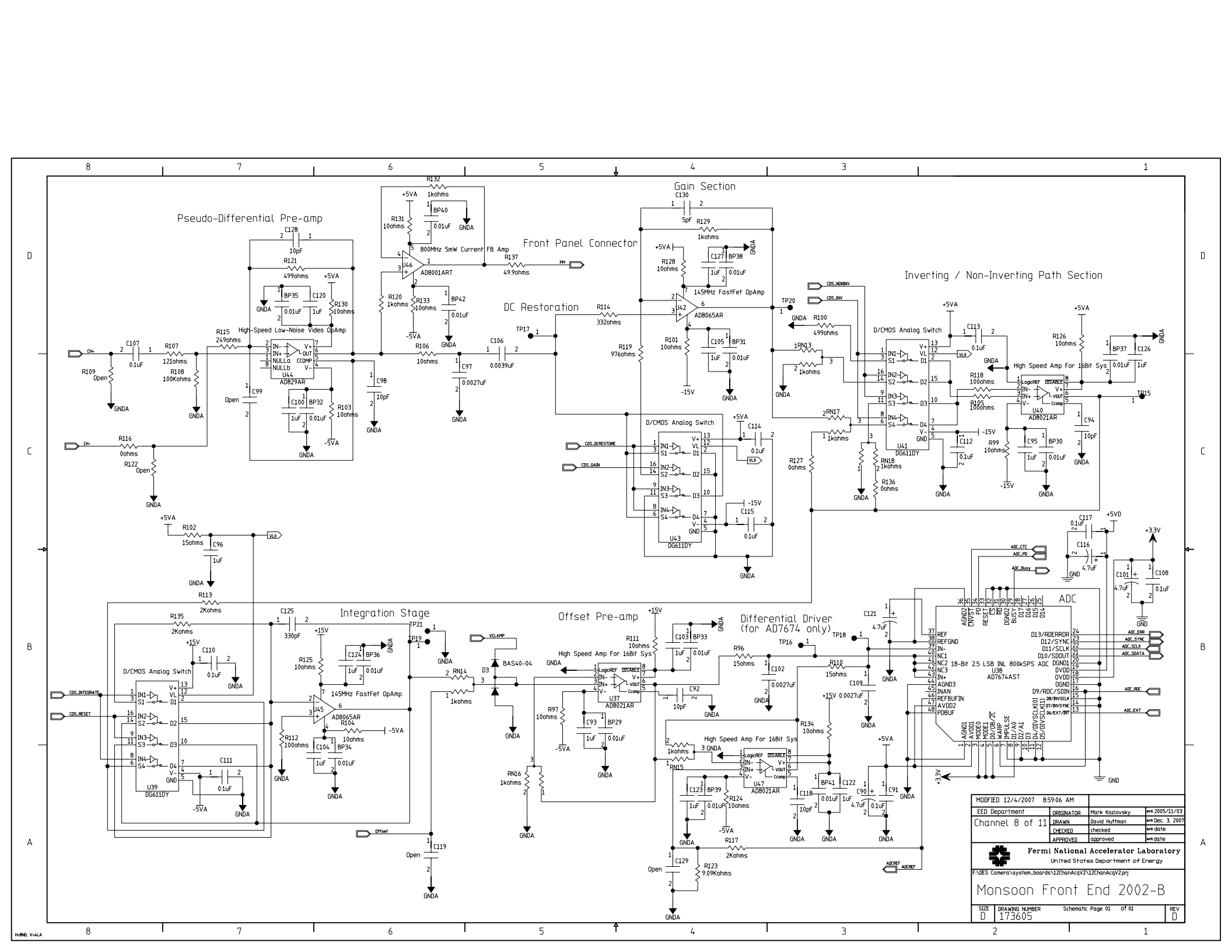

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
Inverting / Non-Inverting Path Section
DC Restoration
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
BAS40-04
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
Monsoon Front End 2002-B
Fermi National Accelerator Laboratory
United States Department of Energy
Channel 2 of 11
EED Department
MODIFIED 12/4/2007 8:59:06 AM
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
SIZE D
DRAWING NUMBER 173605
REV D

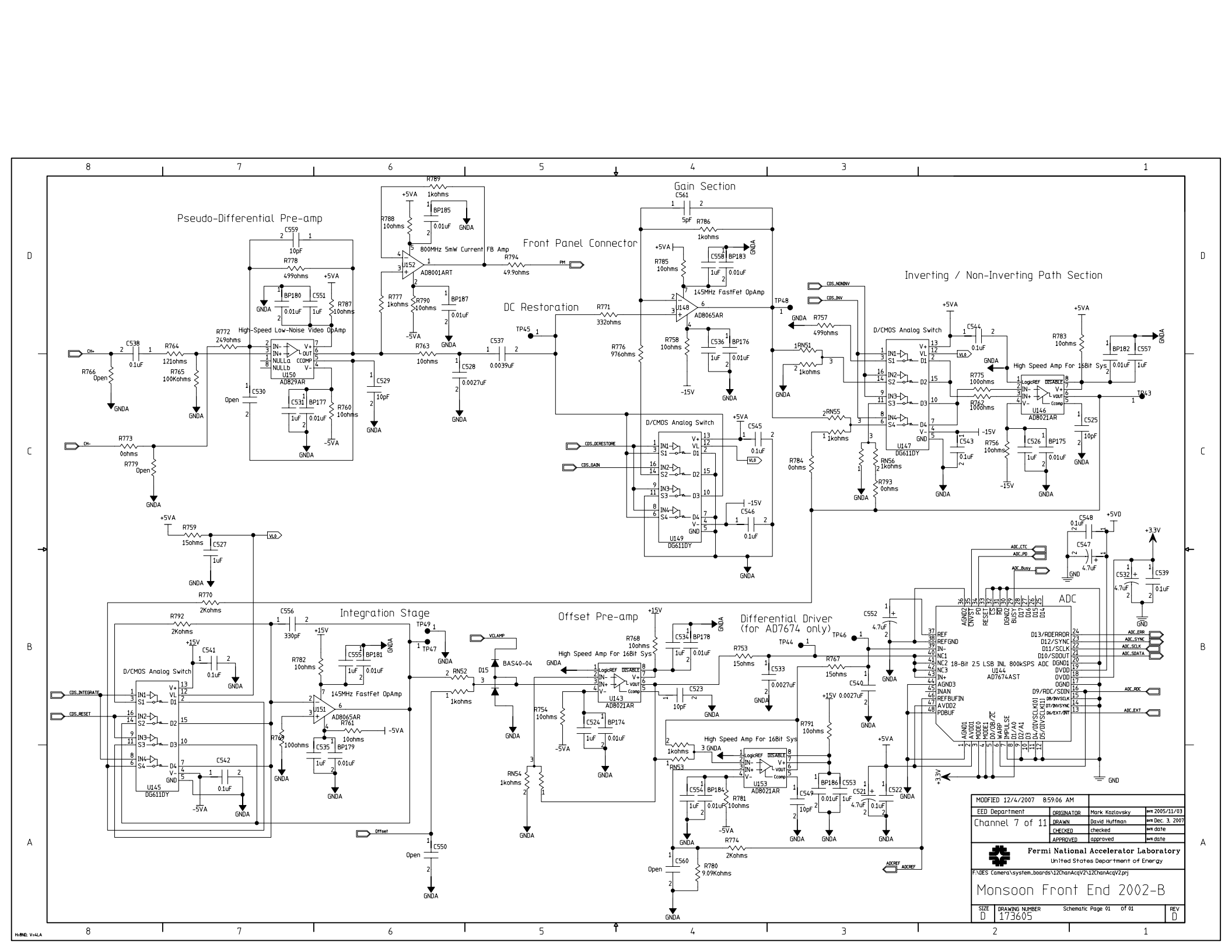

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
Inverting / Non-Inverting Path Section
DC Restoration
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
BAS40-04
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 0 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

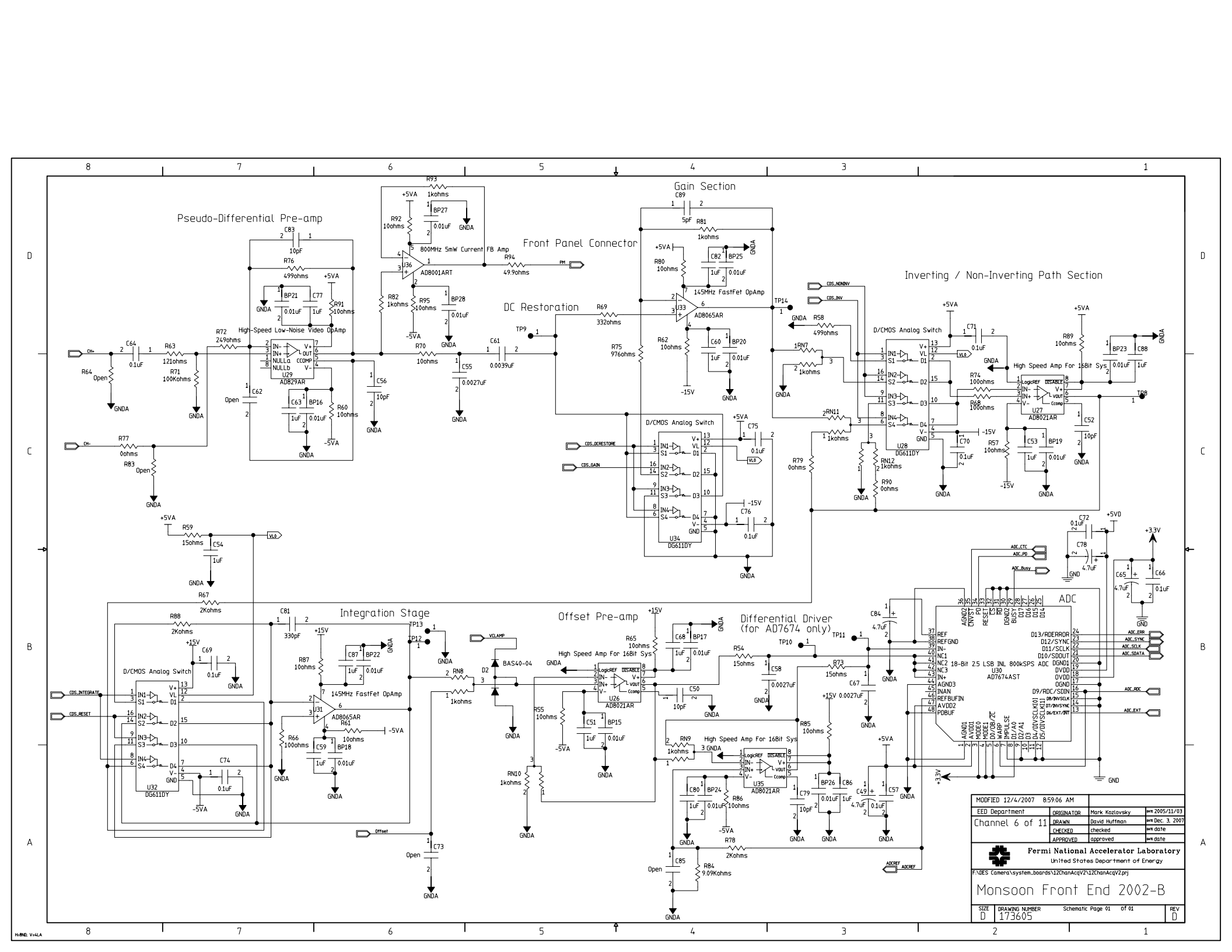

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
Fermi National Accelerator Laboratory
United States Department of Energy
Monsoon Front End 2002-B
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 11 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
DRAWING NUMBER 173605
Schematic Page 01 of 01
SIZE D
REV D

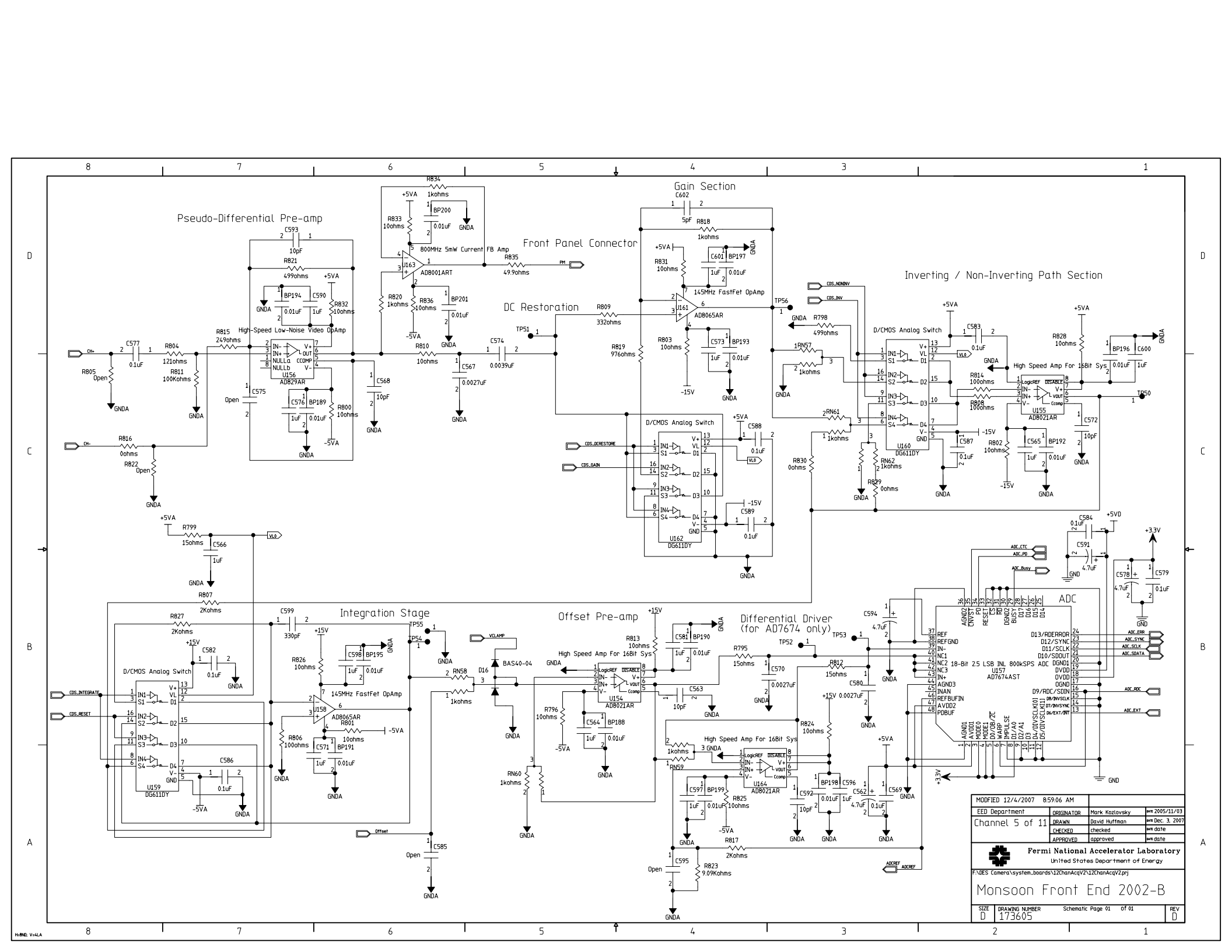

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 10 of 11
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

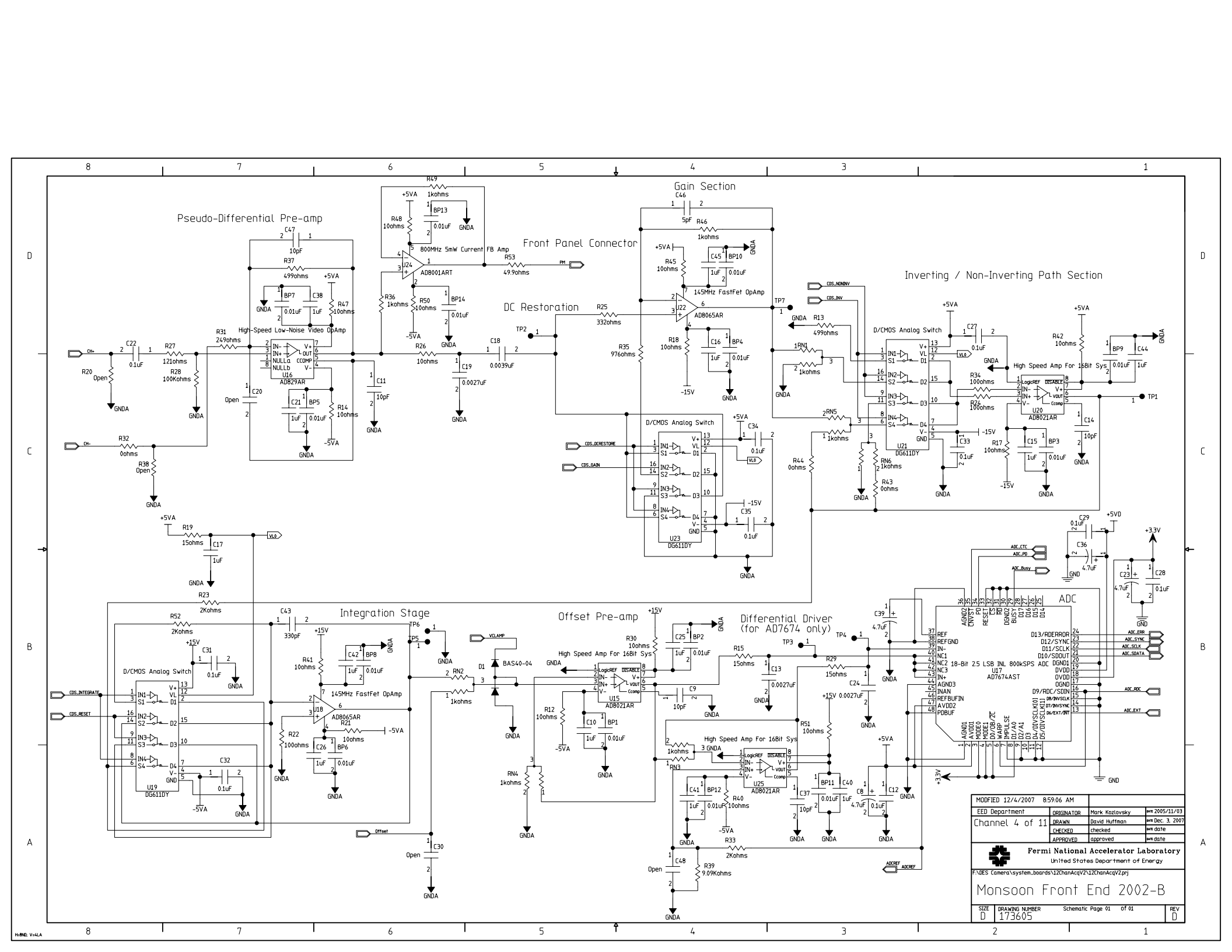

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
Fermi National Accelerator Laboratory
United States Department of Energy
Monsoon Front End 2002-B
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 9 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

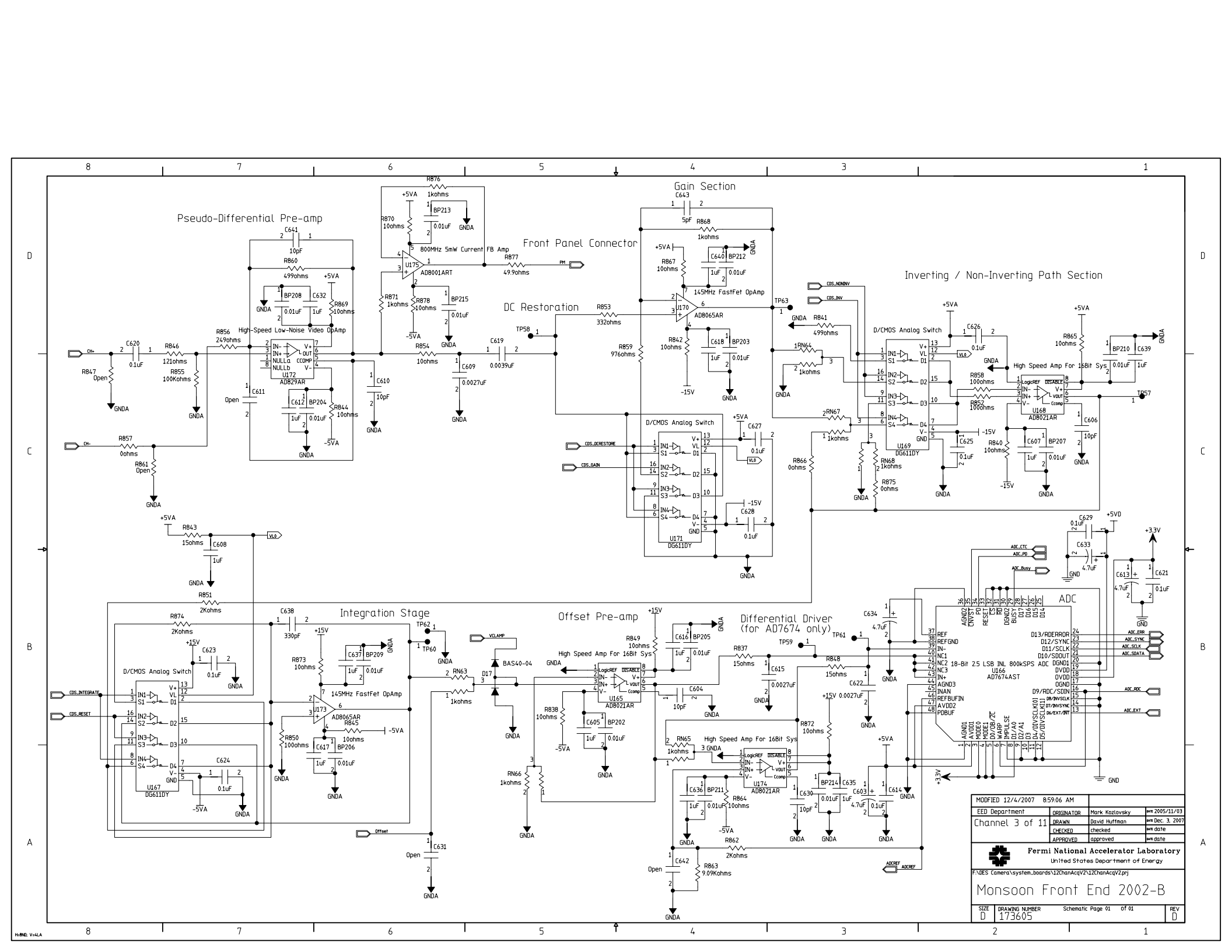

Pseudo-Differential Pre-amp
Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 8 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

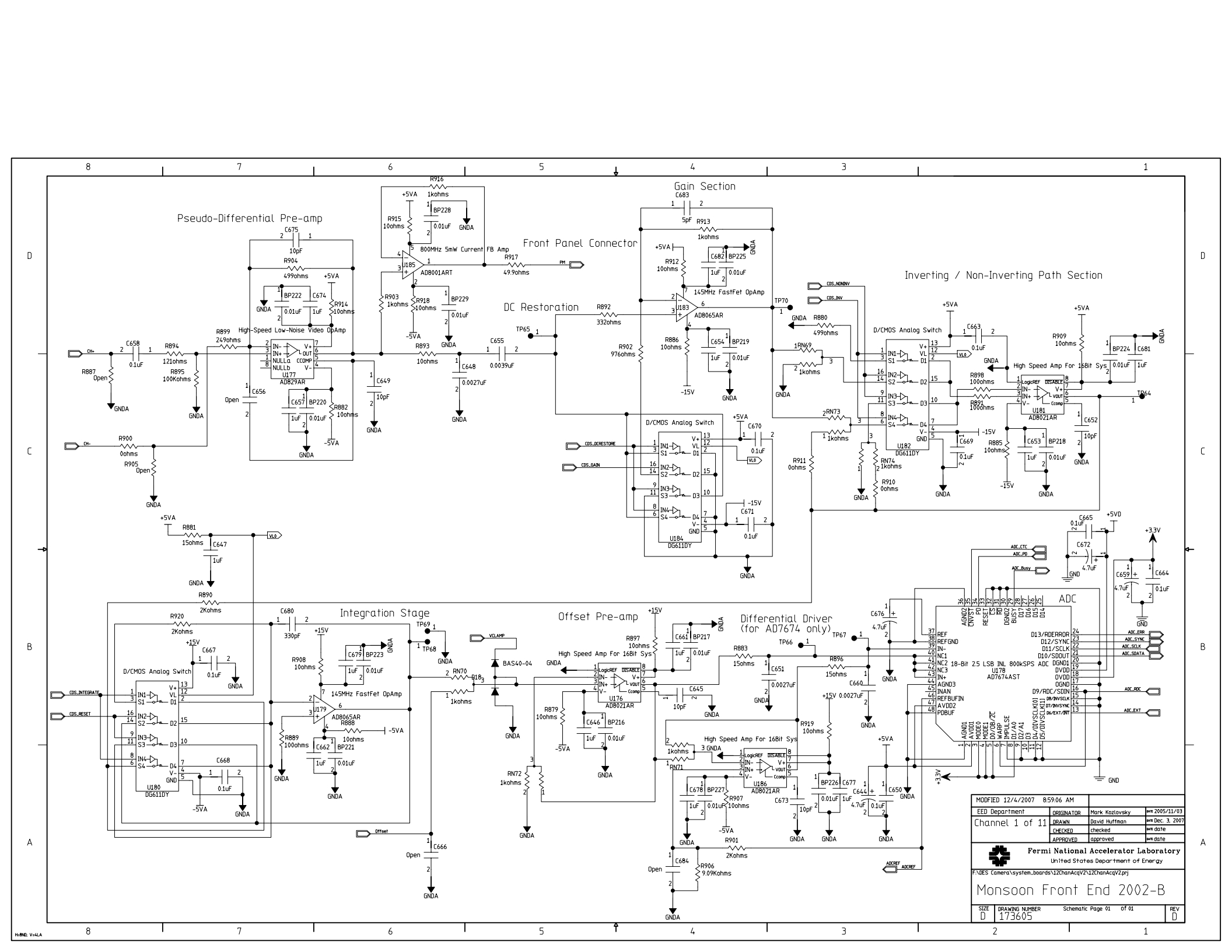

Pseudo-Differential Pre-amp
Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver (for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 7 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

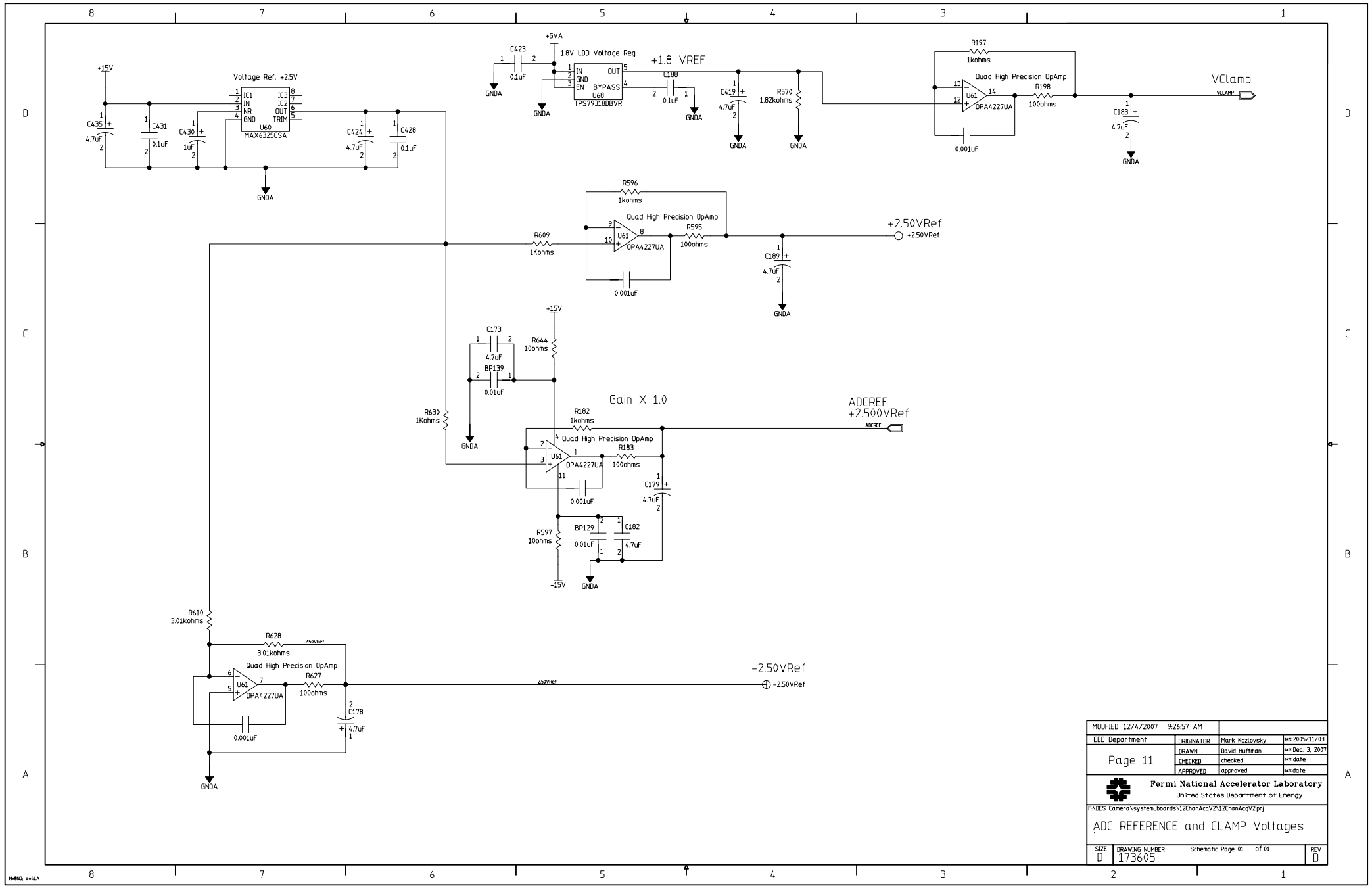

Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 6 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 5 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


Pseudo-Differential Pre-amp
Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 4 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
High-Speed Low-Noise Video OpAmp
18-Bit 2.5 LSB INL 800kSPS ADC
U166
AD7674AST
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 3 of 11
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
800MHz 5mW Current FB Amp
AD8001ART
High-Speed Low-Noise Video OpAmp
AD829AR
145MHz FastFet OpAmp
AD8065AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
MODIFIED 12/4/2007 8:59:06 AM
EED Department
Channel 1 of 11
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



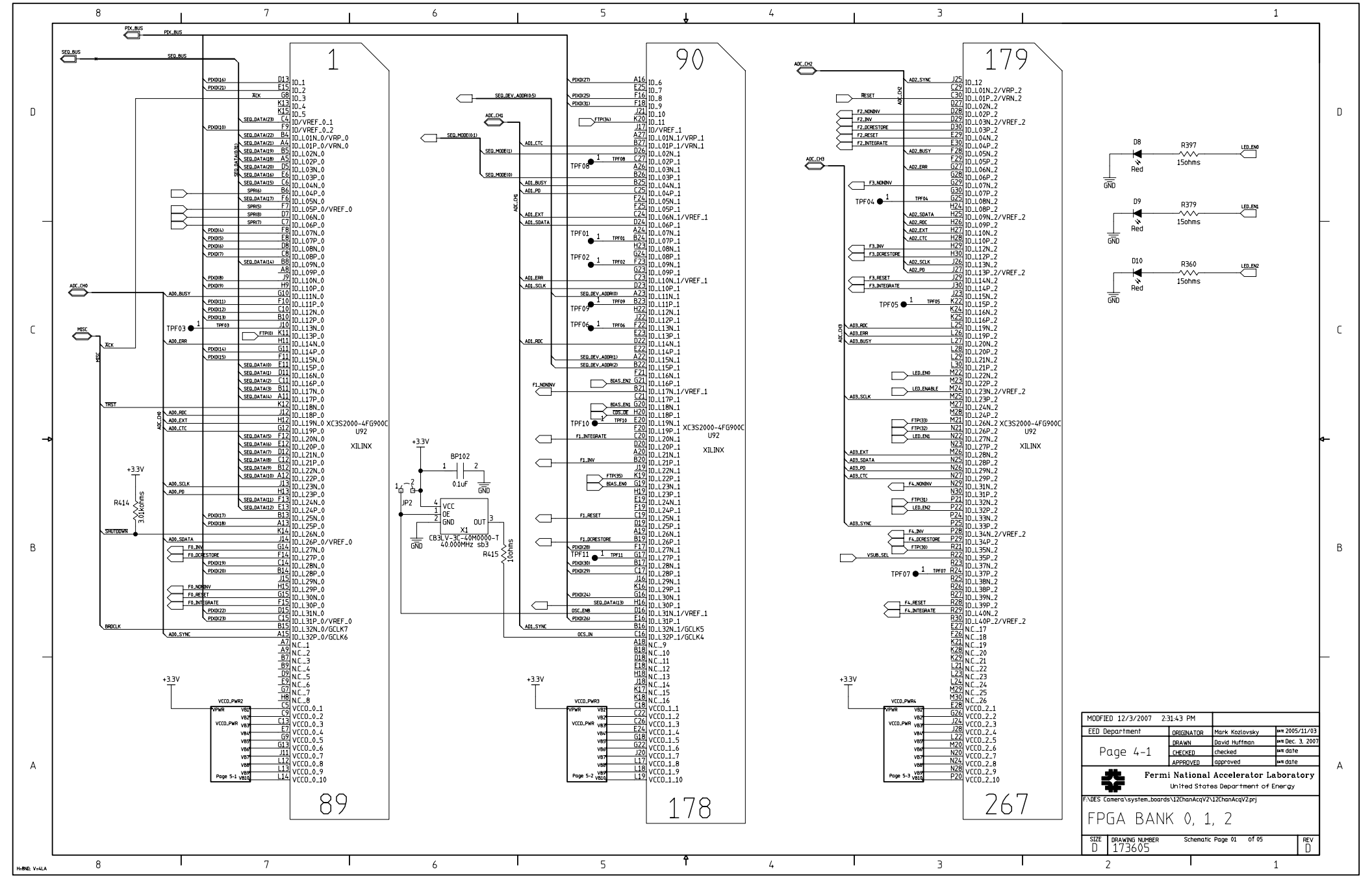
MODFIED 12/4/2007 9:26:57 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 11	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

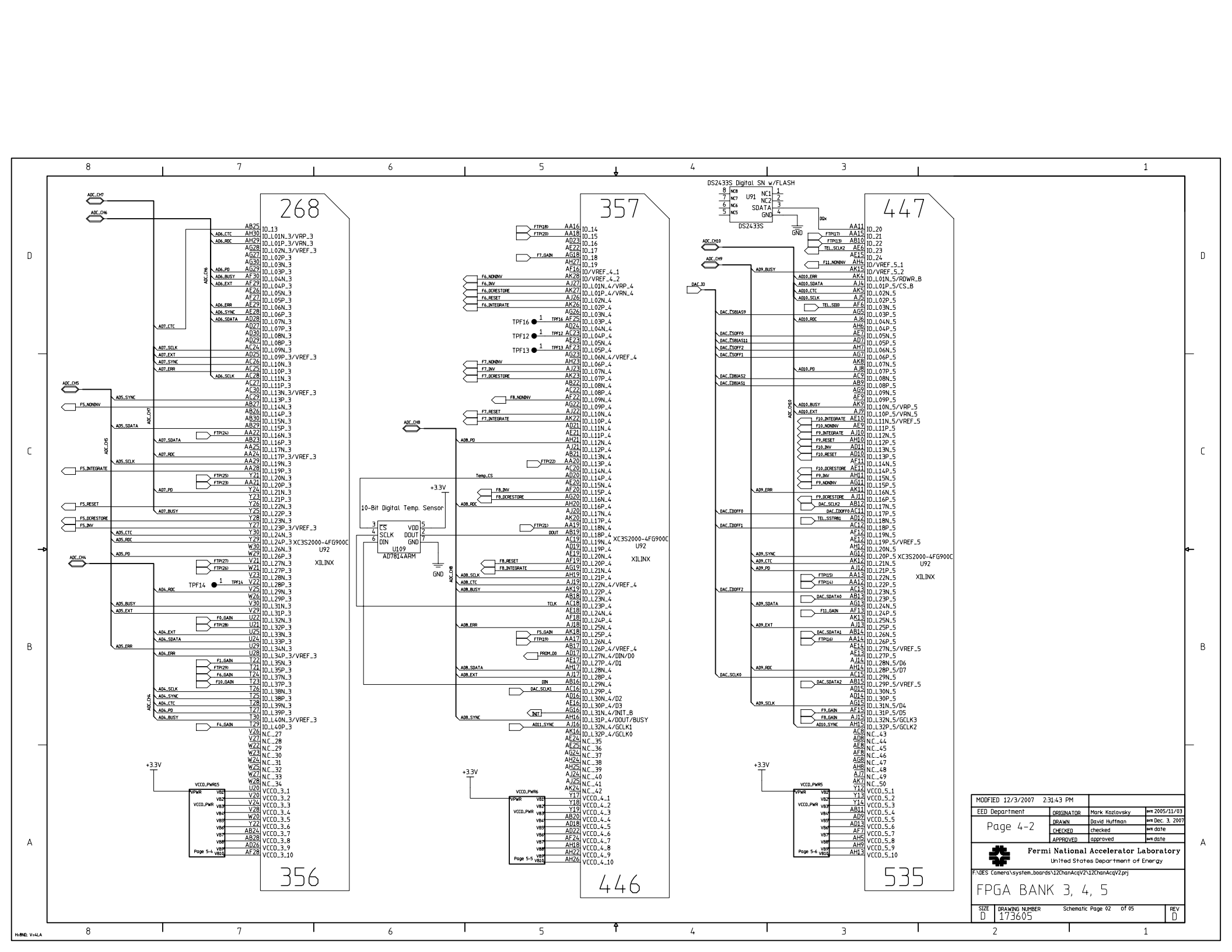
Fermi National Accelerator Laboratory
United States Department of Energy

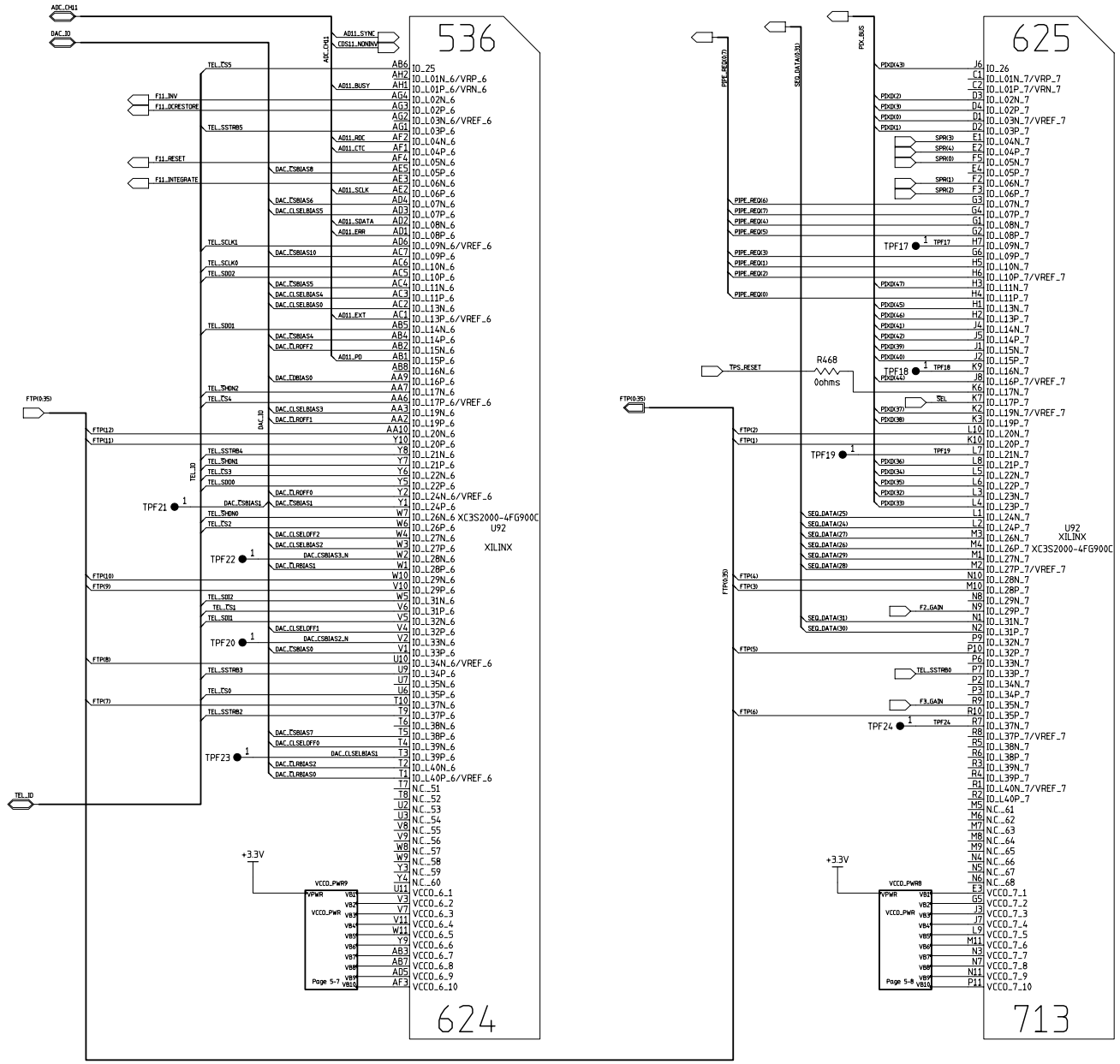
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

ADC REFERENCE and CLAMP Voltages

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D


1
89
90
178
179
267
XC3S2000-4FG900C
U92
XILINX
MODIFIED 12/3/2007 2:31:43 PM
EED Department
Page 4-1
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
FPGA BANK 0, 1, 2
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 05
REV D


268
356
357
446
447
535
XC3S2000-4FG900C
U92
XILINX
10-Bit Digital Temp. Sensor
AD7814ARM
U109
DS2433S Digital SN w/FLASH
DS2433S
U91
FPGA BANK 3, 4, 5
MODIFIED 12/3/2007 2:31:43 PM
EED Department
Page 4-2
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
SIZE D
DRAWING NUMBER 173605
Schematic Page 02 of 05
REV D



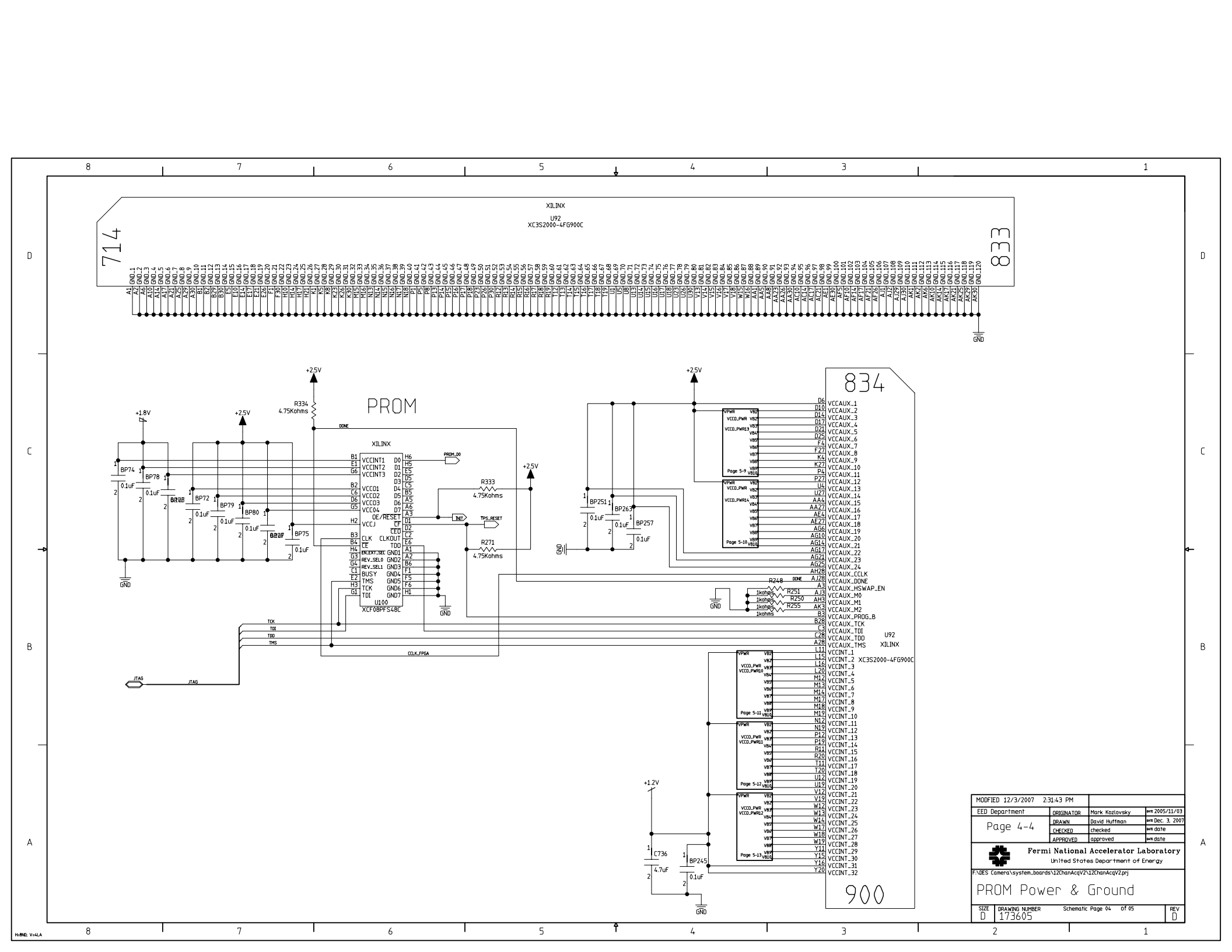
MODIFIED 12/3/2007 2:31:43 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 4-3	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

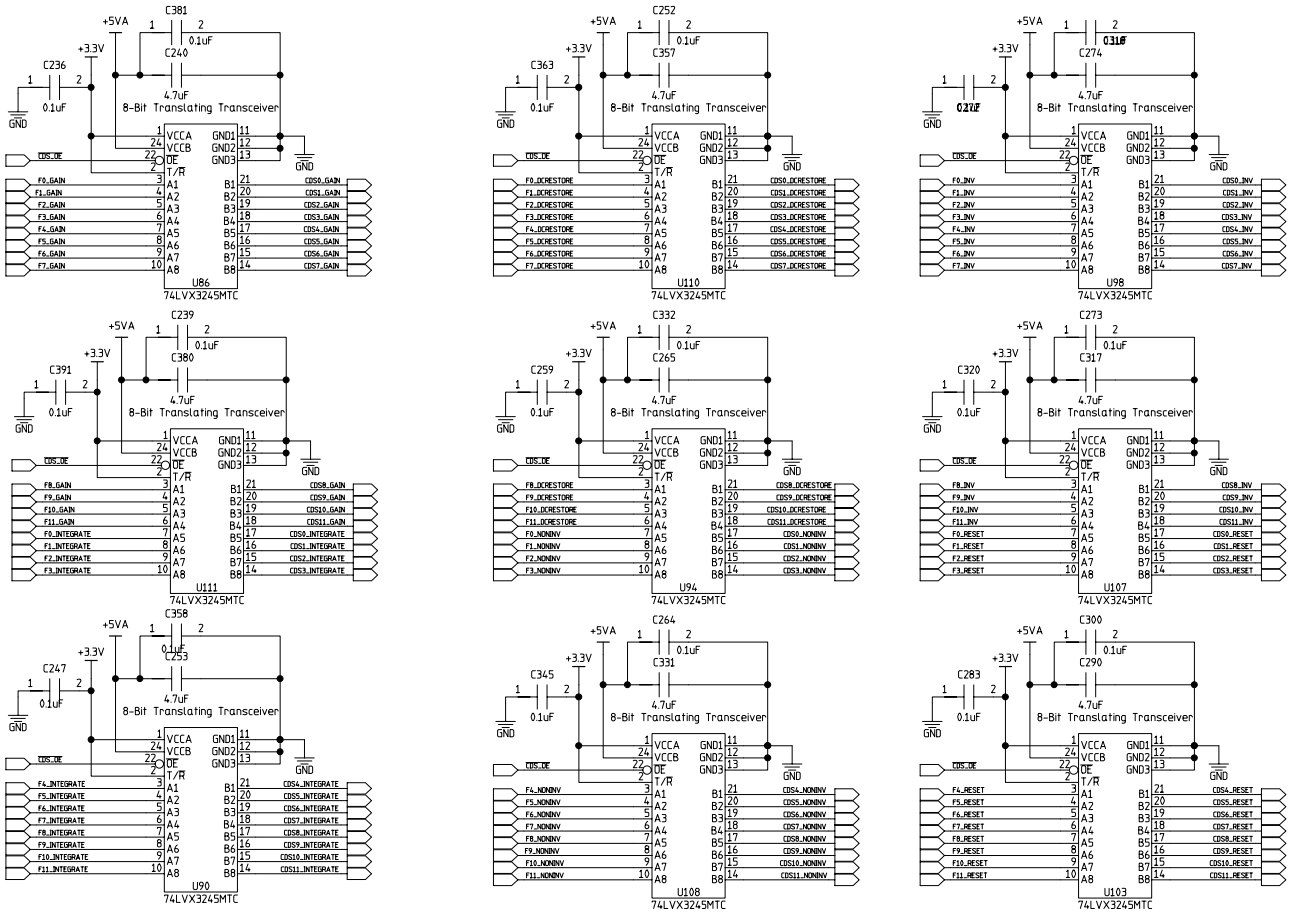
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

FPGA BANK 6, 7

SIZE	DRAWING NUMBER	Schematic Page 03 of 05	REV
D	173605		D


XILINX
U92
XC3S2000-4FG900C
714
833
PROM
XILINX
U100
XCF08PFS48C
R334
4.75Kohms
R333
4.75Kohms
R271
4.75Kohms
R248
R251
R250
R255
1kohms
BP74
BP78
BP72
BP79
BP80
BP75
BP251
BP263
BP257
C736
BP245
0.1uF
4.7uF
+1.8V
+2.5V
+1.2V
GND
DONE
PROM_DO
INIT
TPS_RESET
TCK
TDI
TDO
TMS
CCLK_FPGA
JTAG
834
900
VCCAUX_1
VCCAUX_2
VCCAUX_3
VCCAUX_4
VCCAUX_5
VCCAUX_6
VCCAUX_7
VCCAUX_8
VCCAUX_9
VCCAUX_10
VCCAUX_11
VCCAUX_12
VCCAUX_13
VCCAUX_14
VCCAUX_15
VCCAUX_16
VCCAUX_17
VCCAUX_18
VCCAUX_19
VCCAUX_20
VCCAUX_21
VCCAUX_22
VCCAUX_23
VCCAUX_24
VCCAUX_CCLK
VCCAUX_DONE
VCCAUX_HSWAP_EN
VCCAUX_M0
VCCAUX_M1
VCCAUX_M2
VCCAUX_PROG_B
VCCAUX_TCK
VCCAUX_TDI
VCCAUX_TDO
VCCAUX_TMS
VCCINT_1
VCCINT_2
VCCINT_3
VCCINT_4
VCCINT_5
VCCINT_6
VCCINT_7
VCCINT_8
VCCINT_9
VCCINT_10
VCCINT_11
VCCINT_12
VCCINT_13
VCCINT_14
VCCINT_15
VCCINT_16
VCCINT_17
VCCINT_18
VCCINT_19
VCCINT_20
VCCINT_21
VCCINT_22
VCCINT_23
VCCINT_24
VCCINT_25
VCCINT_26
VCCINT_27
VCCINT_28
VCCINT_29
VCCINT_30
VCCINT_31
VCCINT_32
U92
XILINX
XC3S2000-4FG900C
MODIFIED 12/3/2007 2:31:43 PM
EED Department
Page 4-4
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
PROM Power & Ground
SIZE D
DRAWING NUMBER 173605
Schematic Page 04 of 05
REV D



MODIFIED 12/3/2007 2:31:43 PM

EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 4-5	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

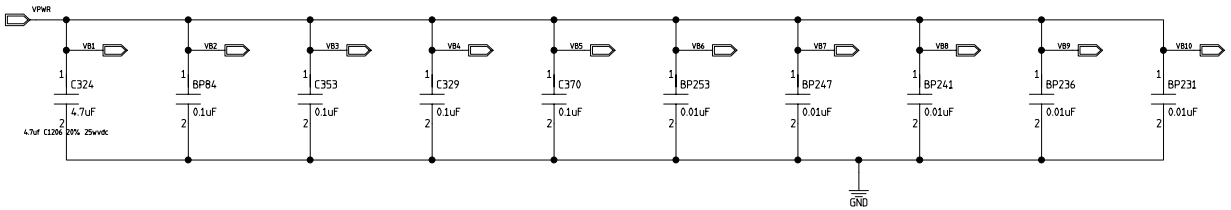
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Level Translators

SIZE	DRAWING NUMBER	Schematic Page 05 of 05	REV
D	173605		D

H=END: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-9	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

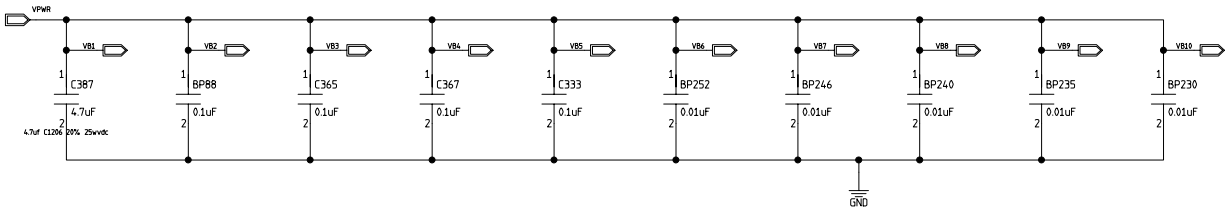
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -10	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

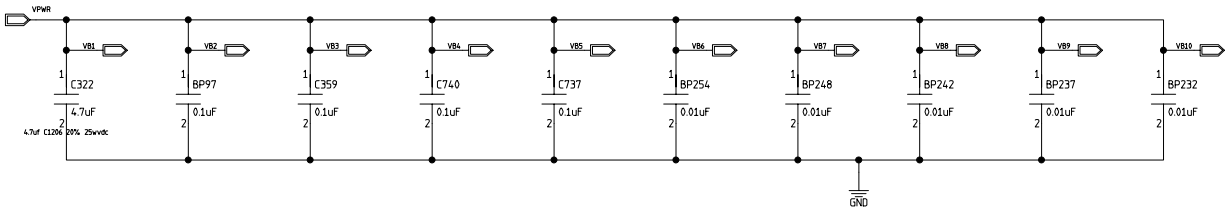
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-13	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

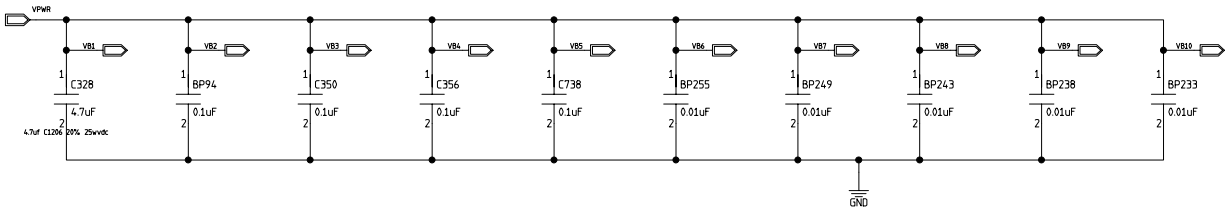
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-12	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

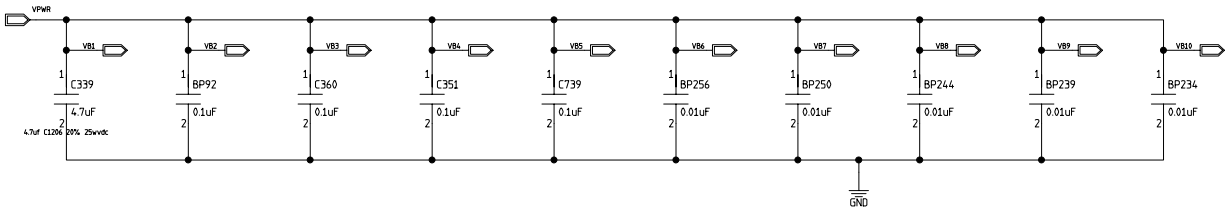
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -11	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

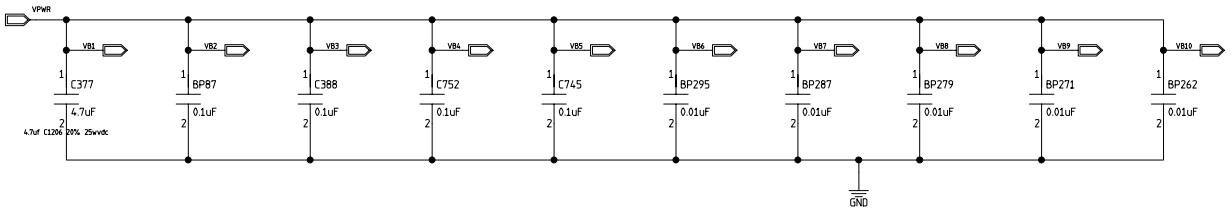
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=GND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-7	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

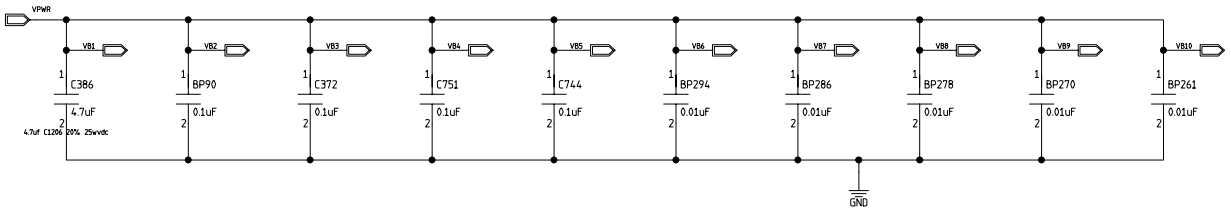
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-8	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

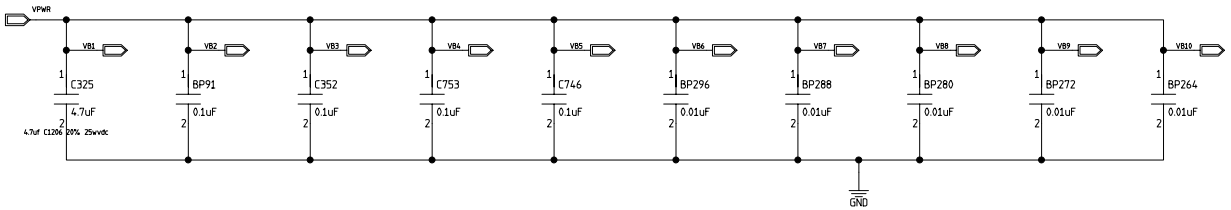
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-4	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

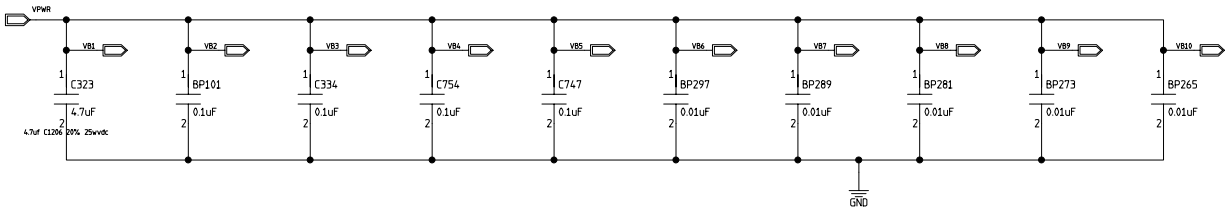
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -5	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

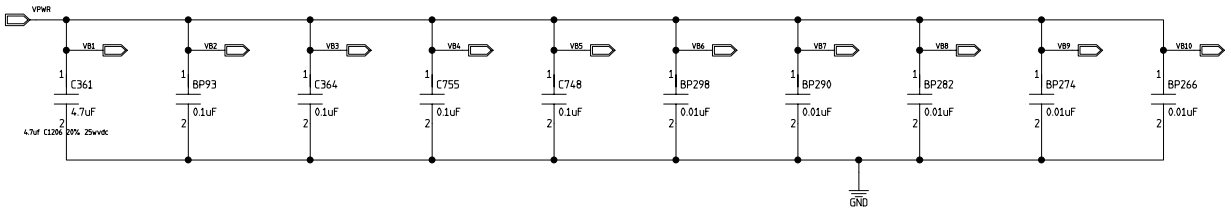
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -6	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

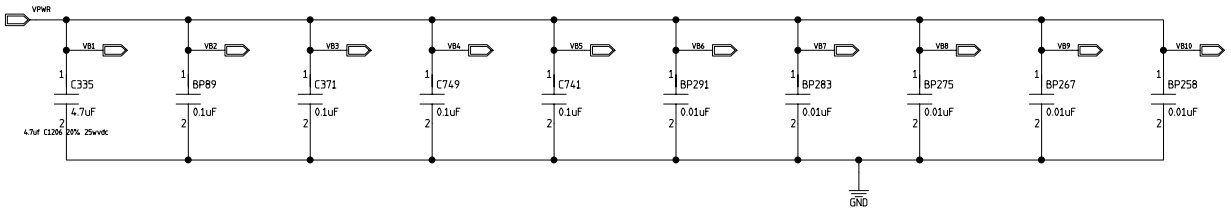
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5-3	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

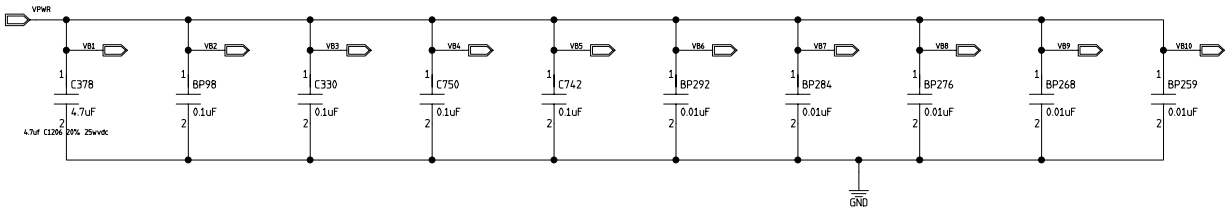
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D

H=BND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -2	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

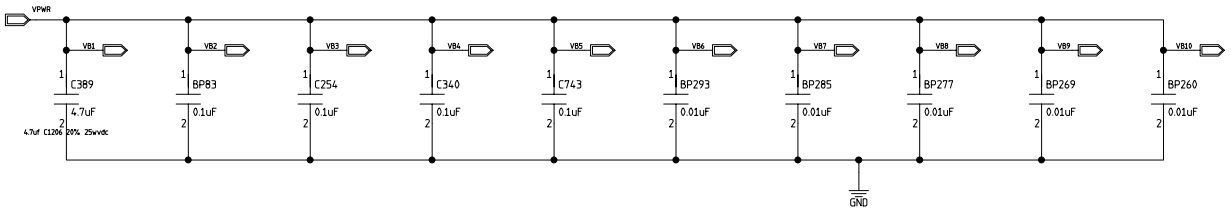
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=GND: V=4LA



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 5 -1	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

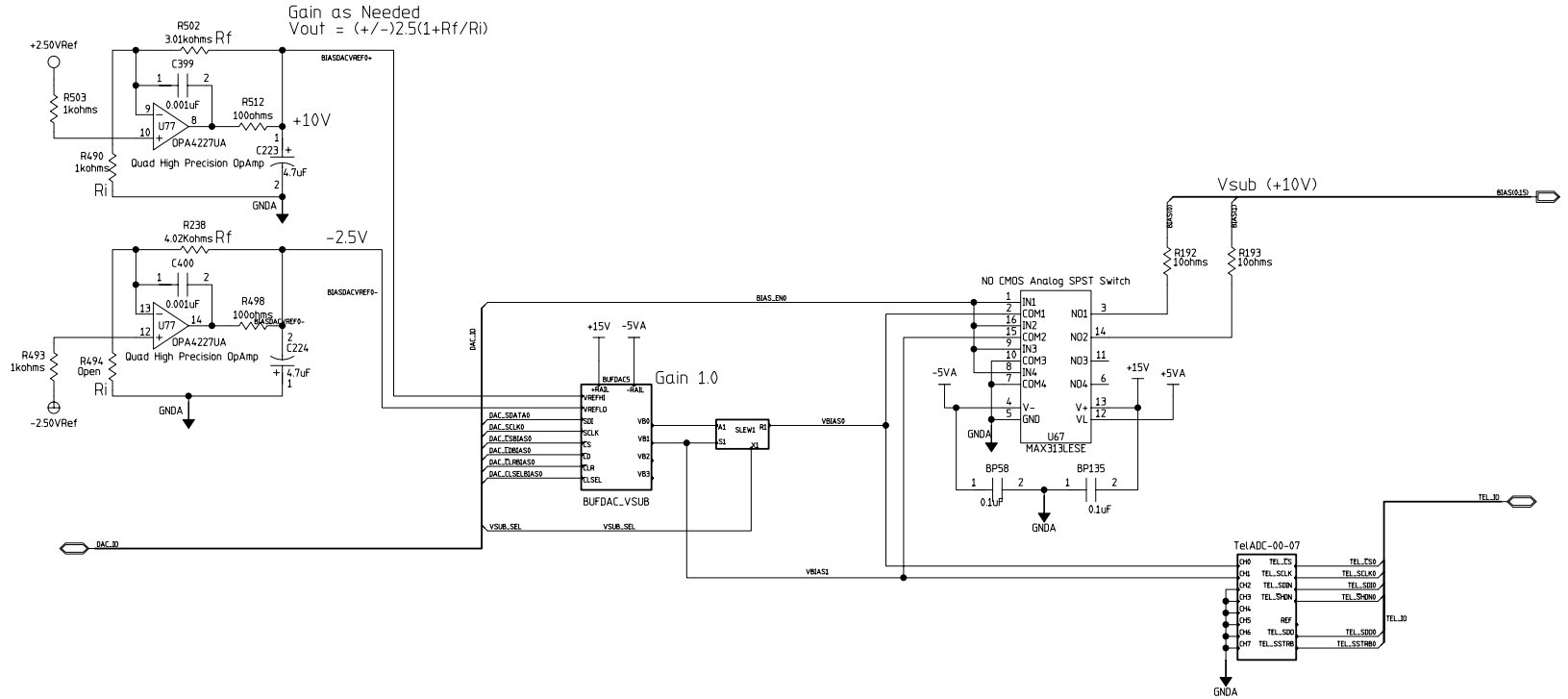
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Power Rail By-Passing

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=BND: V=4LA



Vsub CHANNELS 0-1
WRITE Memory Location 0x220-221
READ Memory Location 0x440-441

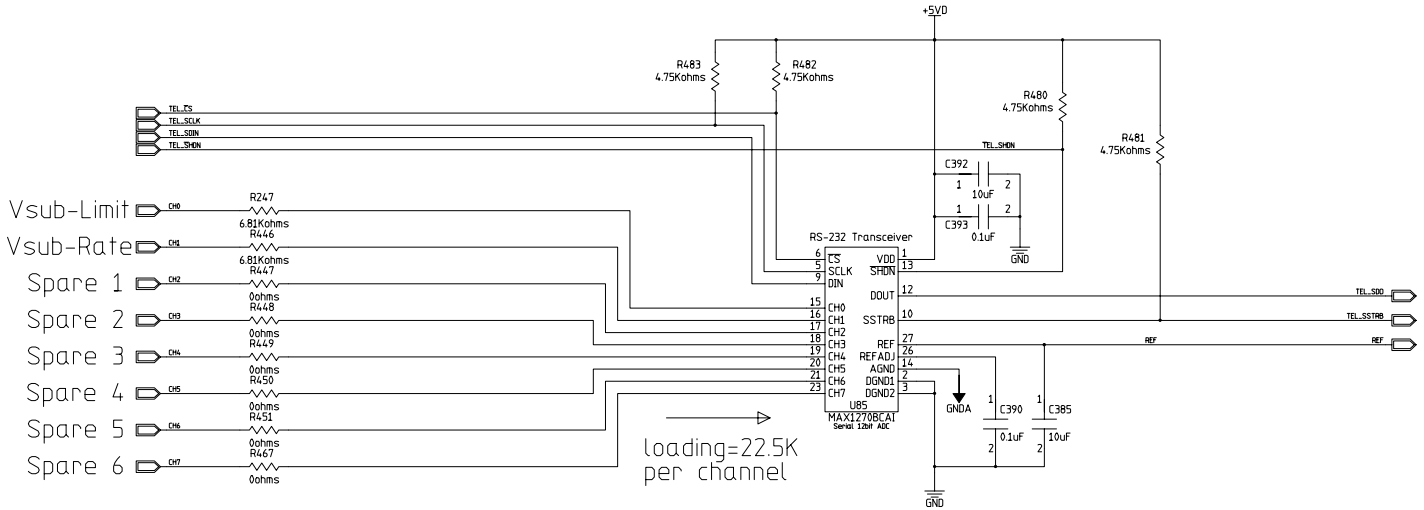
MODFIED 12/7/2007 9:13:07 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 9	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Bias Output w/Enable 1-16

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D



TELEMETRY CHANNELS BIAS 0-7
READ Memory Location 0x440-447

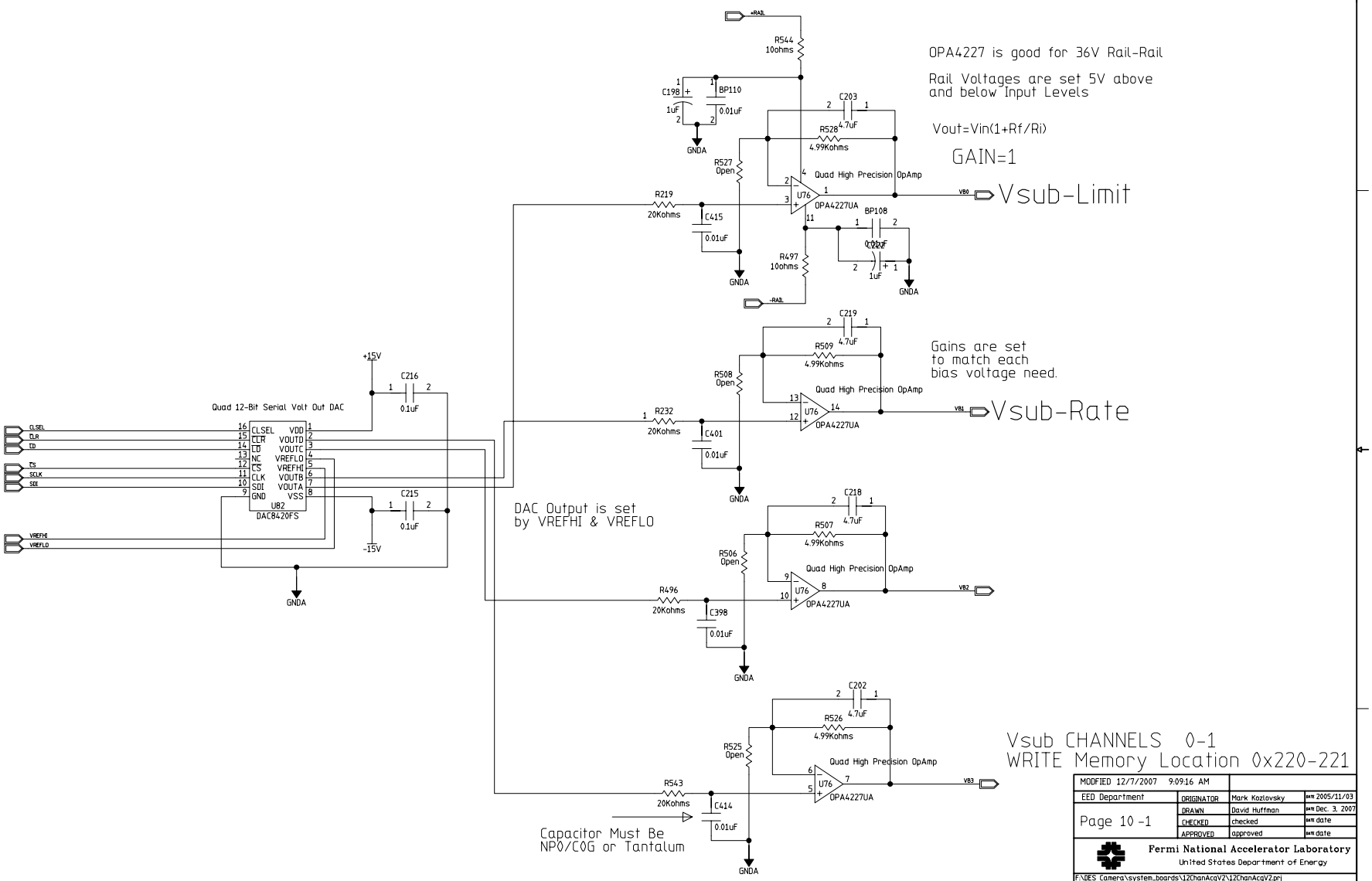
MODFIED 12/7/2007 9:02:36 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

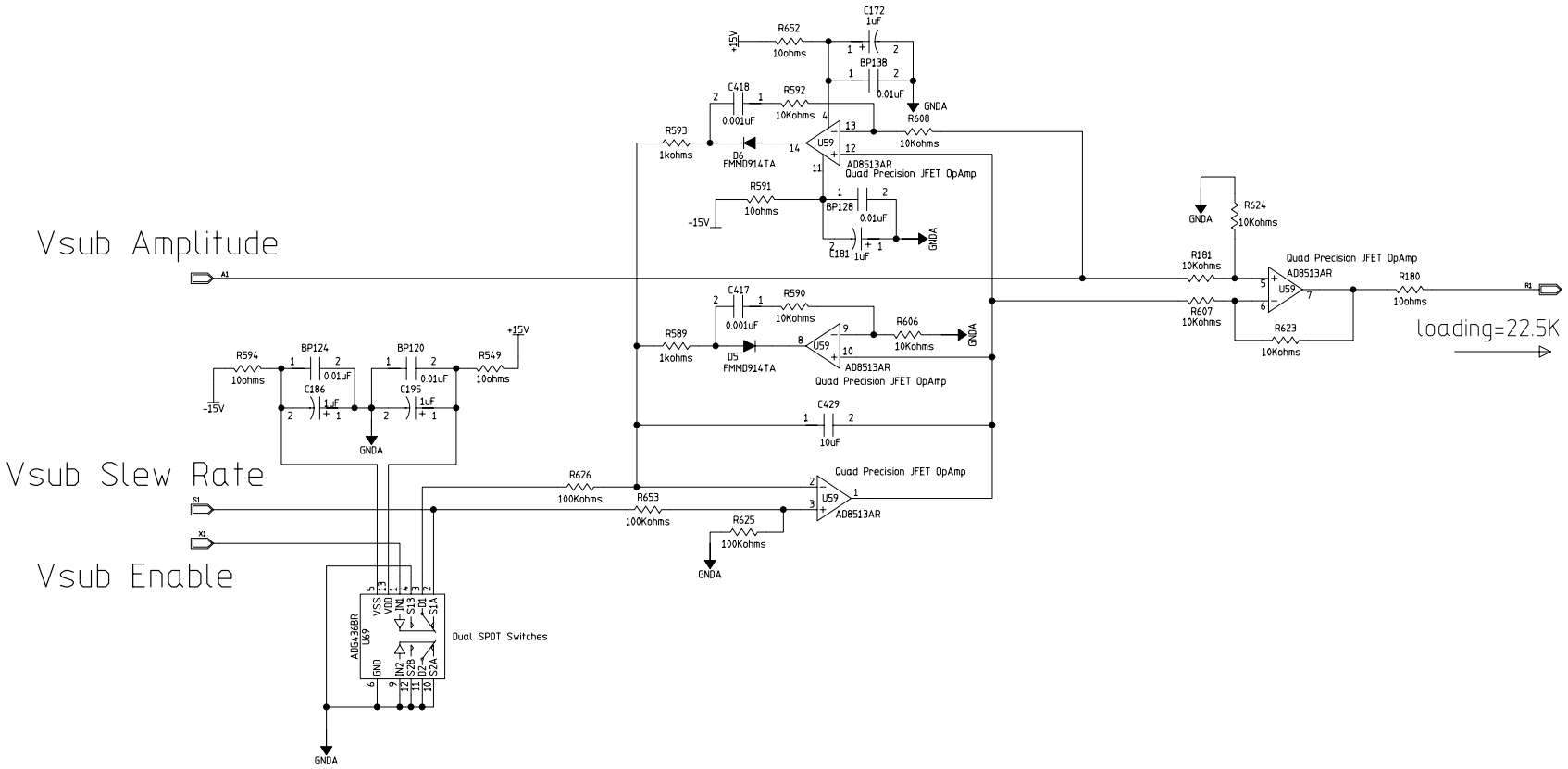
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

TelADC 0-7

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D


OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1
Vsub-Limit
Gains are set to match each bias voltage need.
Vsub-Rate
DAC Output is set by VREFHI & VREFLO
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
Quad High Precision OpAmp
OPA4227UA
Capacitor Must Be NP0/C0G or Tantalum
Vsub CHANNELS 0-1
WRITE Memory Location 0x220-221
Page 10 -1
Fermi National Accelerator Laboratory
United States Department of Energy
4 Channel Buffered DAC - VSUB Ramp Control
BIAS 0,1
DRAWING NUMBER 173605
Schematic Page 01 of 01



Vsub Limit & Rate
WRITE Memory Location 0x220-221

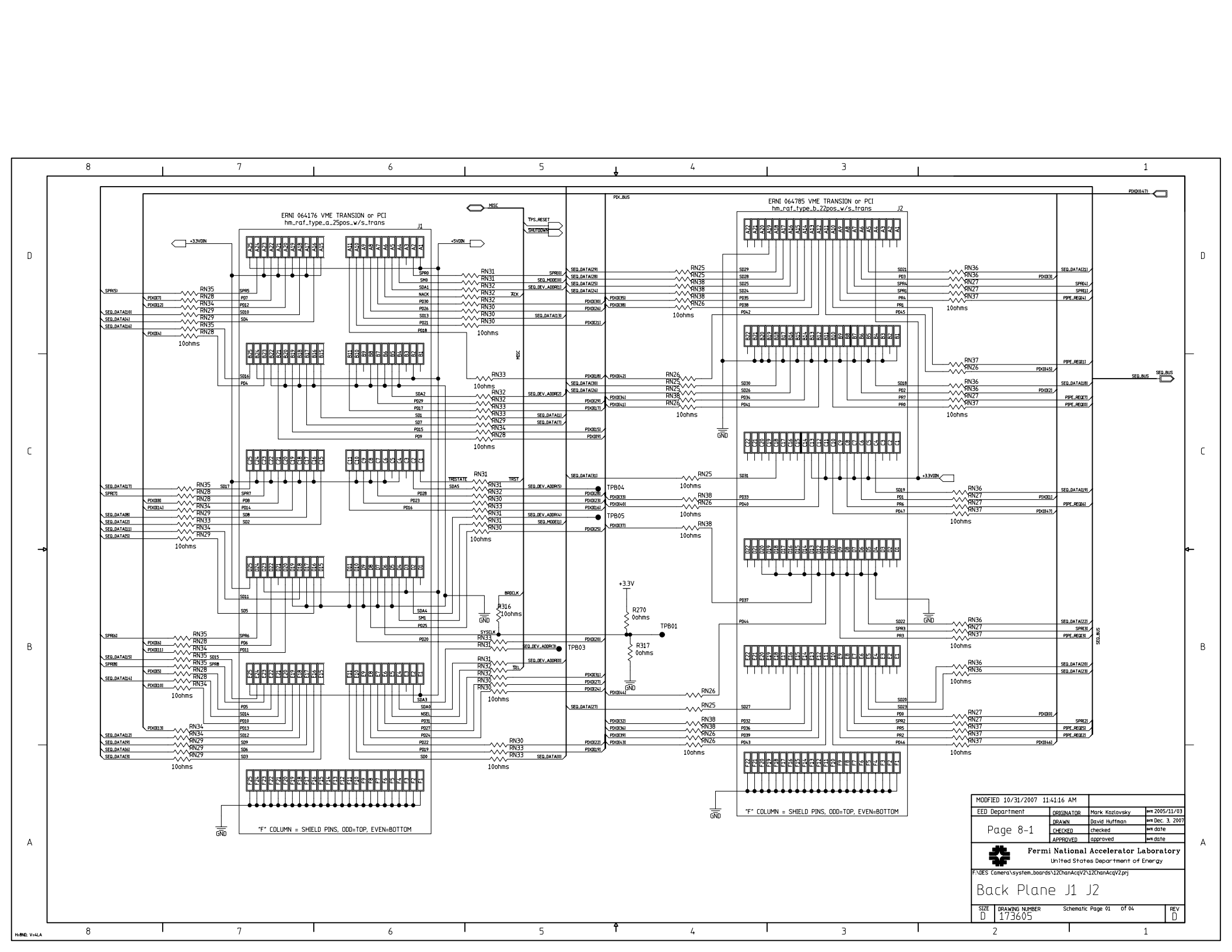
MODIFIED 12/7/2007 9:11:05 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 17	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

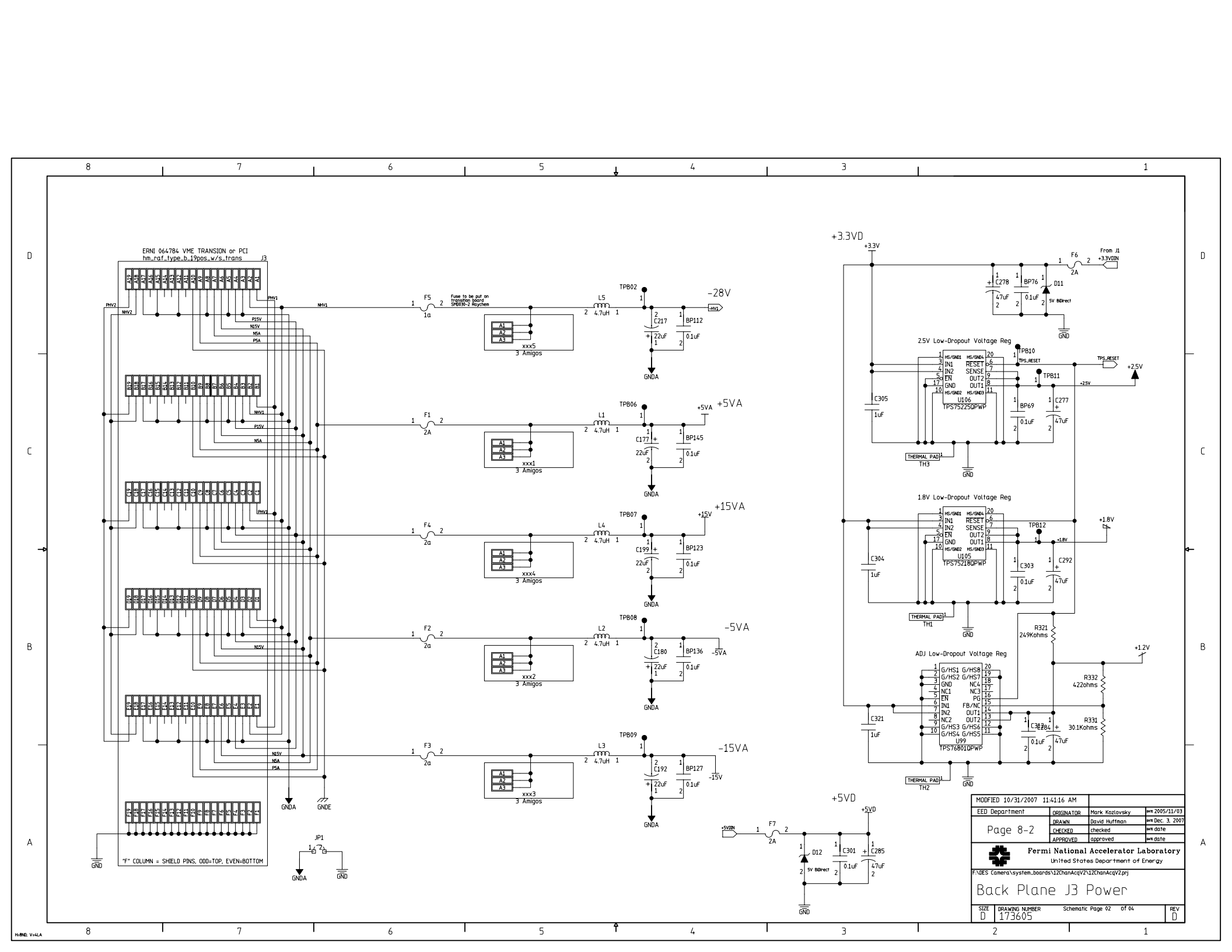
Fermi National Accelerator Laboratory
United States Department of Energy

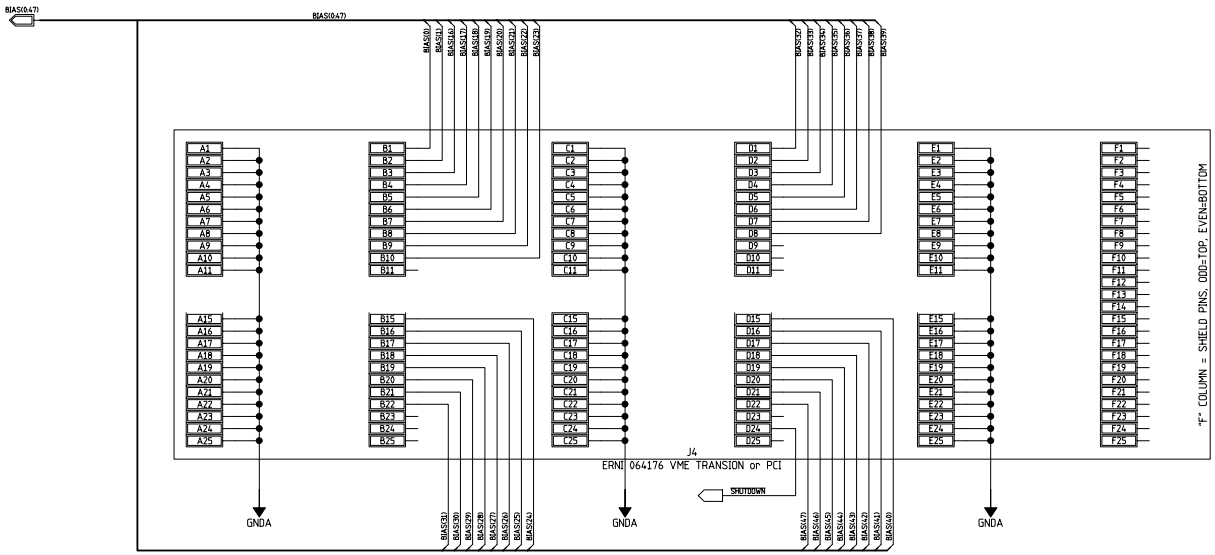
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

SLEW CONTROL

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D


ERNI 064176 VME TRANSION or PCI
hm_raf_type_a_25pos_w/s_trans
J1
ERNI 064785 VME TRANSION or PCI
hm_raf_type_b_22pos_w/s_trans
J2
PIX_BUS
MISC
TPS_RESET
SHUTDOWN
+3.3VDIN
+5VDIN
10ohms
GND
+3.3V
TPB01
TPB03
TPB04
TPB05
R270 0ohms
R316 10ohms
R317 0ohms
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
SEQ_BUS
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Back Plane J1 J2
MODIFIED 10/31/2007 11:41:16 AM
EED Department
Page 8-1
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 04
REV D


ERNI 064784 VME TRANSION or PCI
hm_raf_type_b_19pos_w/s_trans
J3
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
PHV1
PHV2
NHV1
NHV2
P15V
N15V
N5A
P5A
GNDA
GNDE
GND
JP1
F5
1a
Fuse to be put on transition board SMD030-2 Raychem
L5
4.7uH
TPB02
-28V
-HV1
C217
22uF
BP112
0.1uF
xxx5
3 Amigos
F1
2A
L1
4.7uH
TPB06
+5VA
C177
22uF
BP145
xxx1
F4
2a
L4
TPB07
+15VA
+15V
C199
BP123
xxx4
F2
L2
TPB08
-5VA
C180
BP136
xxx2
F3
L3
TPB09
-15VA
-15V
C192
BP127
xxx3
+3.3VD
+3.3V
From J1
+3.3VDIN
F6
2A
C278
47uF
BP76
0.1uF
D11
5V BODirect
2.5V Low-Dropout Voltage Reg
U106
TPS75225QPWP
TPB10
TPS_RESET
TPB11
+2.5V
C305
1uF
BP69
C277
1.8V Low-Dropout Voltage Reg
U105
TPS75218QPWP
TPB12
+1.8V
C304
C303
C292
THERMAL PAD
TH3
TH1
R321
249Kohms
+1.2V
ADJ Low-Dropout Voltage Reg
U99
TPS76801QPWP
R332
422ohms
R331
30.1Kohms
C321
C284
+5VD
+5VDIN
F7
2A
D12
C301
C285
TH2
MODIFIED 10/31/2007 11:41:16 AM
EED Department
Page 8-2
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Back Plane J3 Power
SIZE D
DRAWING NUMBER 173605
Schematic Page 02 of 04
REV D



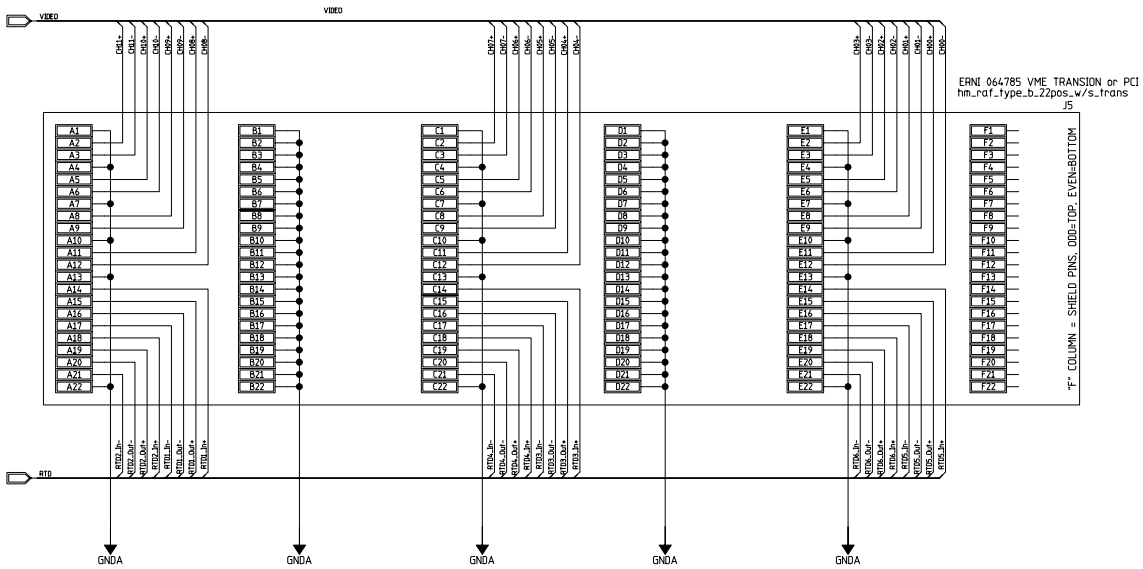
MODIFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 8-3	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

DIGITAL OUTPUTS & BIAS J4

SIZE	DRAWING NUMBER	Schematic Page 03 of 04	REV
D	173605		D



MODFIED 10/31/2007 11:41:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 8-4	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

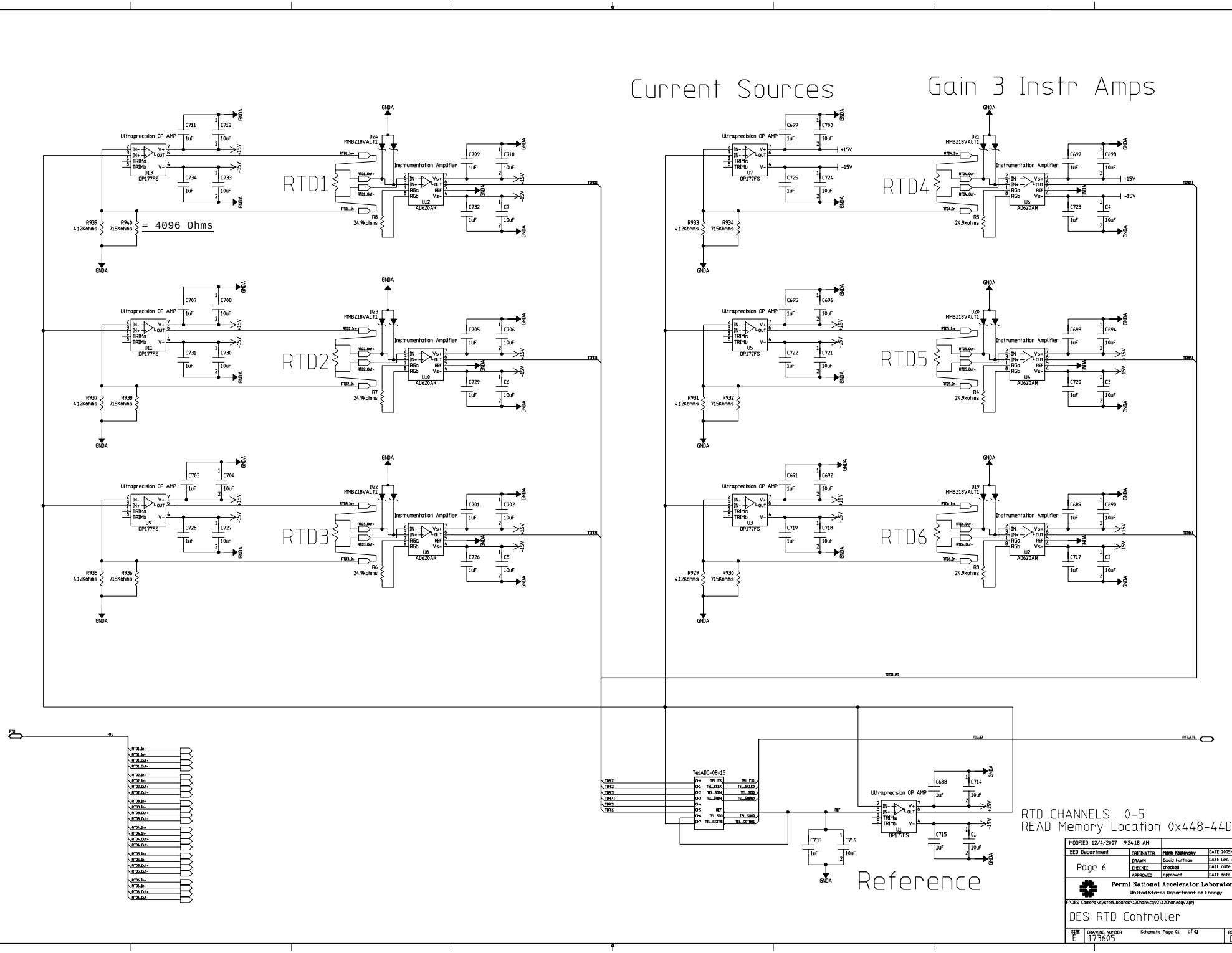
Fermi National Accelerator Laboratory
United States Department of Energy

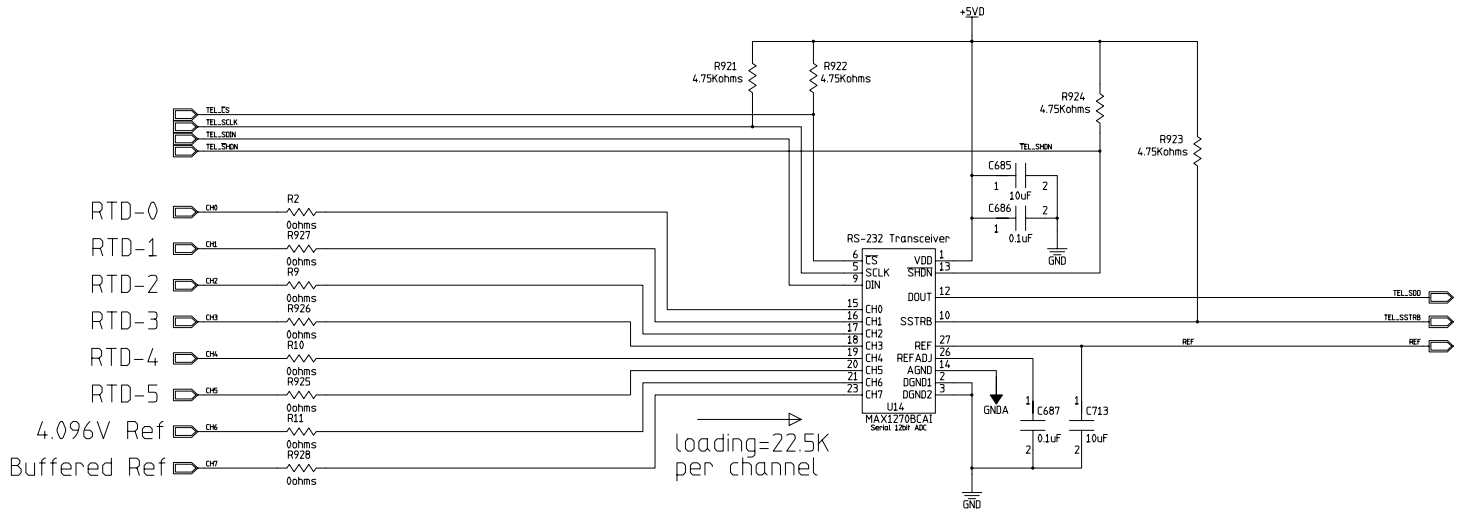
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

VIDEO INPUTS & RTD INPUTS J5

SIZE	DRAWING NUMBER	Schematic Page 04 of 04	REV
D	173605		D

H=BND: V=4LA


Current Sources
Gain 3 Instr Amps
RTD1
RTD2
RTD3
RTD4
RTD5
RTD6
= 4096 Ohms
Reference
RTD CHANNELS 0-5
READ Memory Location 0x448-44D
DES RTD Controller
Fermi National Accelerator Laboratory
United States Department of Energy
Page 6
MODIFIED 12/4/2007 9:24:18 AM
EED Department
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Dec. 3, 2007
CHECKED checked DATE date
APPROVED approved DATE date
SIZE E
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



READ Memory Location 0x448-44F

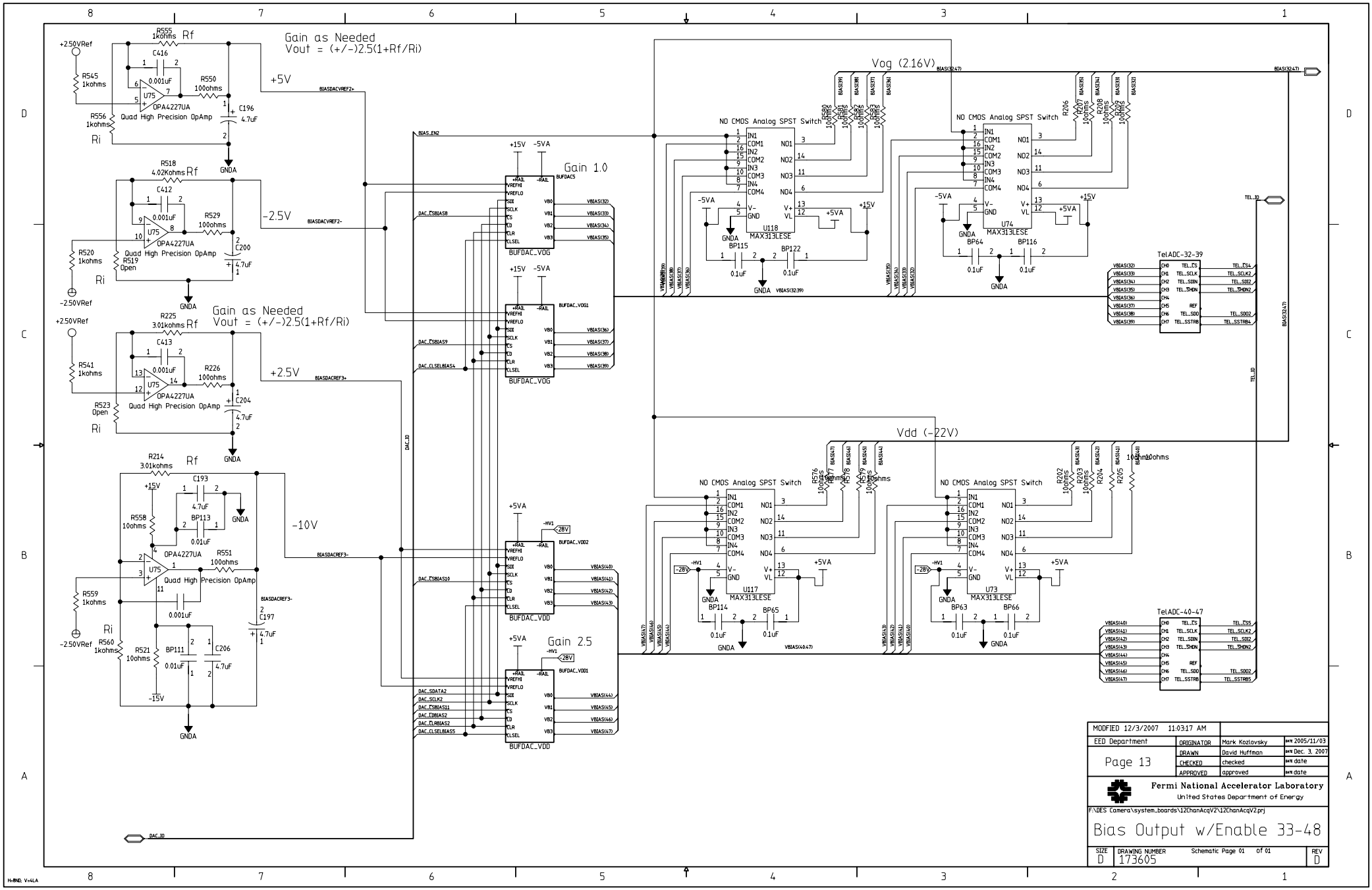
MODFIED 12/7/2007 9:01:21 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

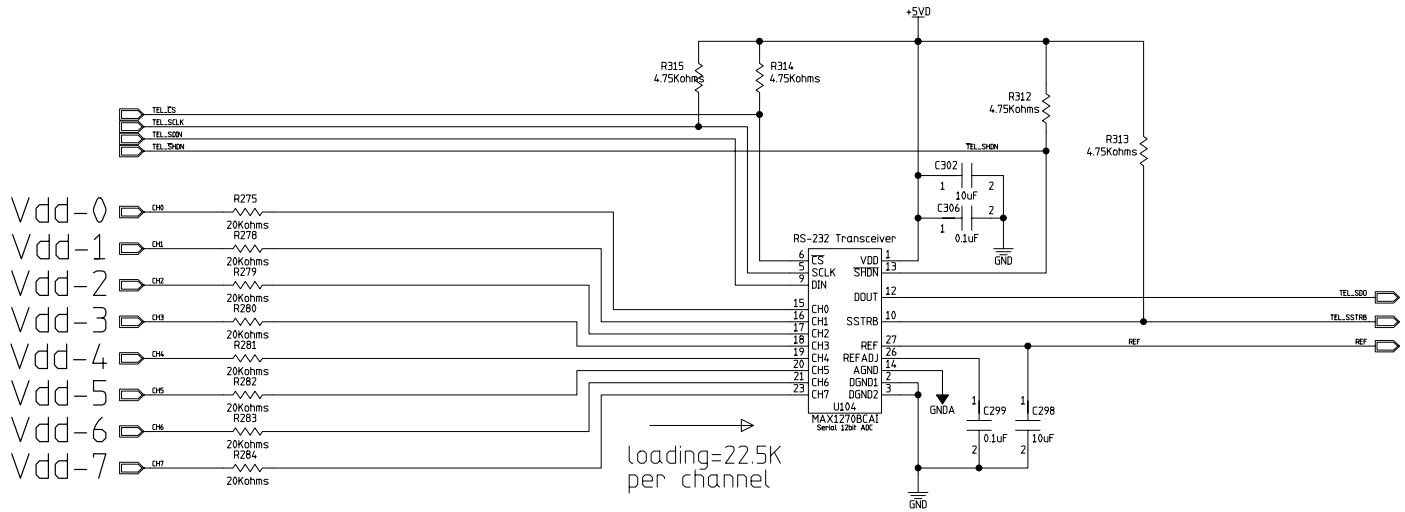
Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

TelADC 8-15

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		D


Gain as Needed
Vout = (+/-)2.5(1+Rf/Ri)
+2.50VRef
-2.50VRef
+5V
-2.5V
+2.5V
-10V
Quad High Precision OpAmp
OPA4227UA
Gain 1.0
Gain 2.5
Vog (2.16V)
Vdd (-22V)
NO CMOS Analog SPST Switch
MAX313LESE
BUFDAC_VOG
BUFDAC_VOG1
BUFDAC_VDD2
BUFDAC_VDD1
TelADC-32-39
TelADC-40-47
MODIFIED 12/3/2007 11:03:17 AM
EED Department
Page 13
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
Bias Output w/Enable 33-48
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D



TELEMETRY CHANNELS BIAS 40-47
READ Memory Location 0x468-46F

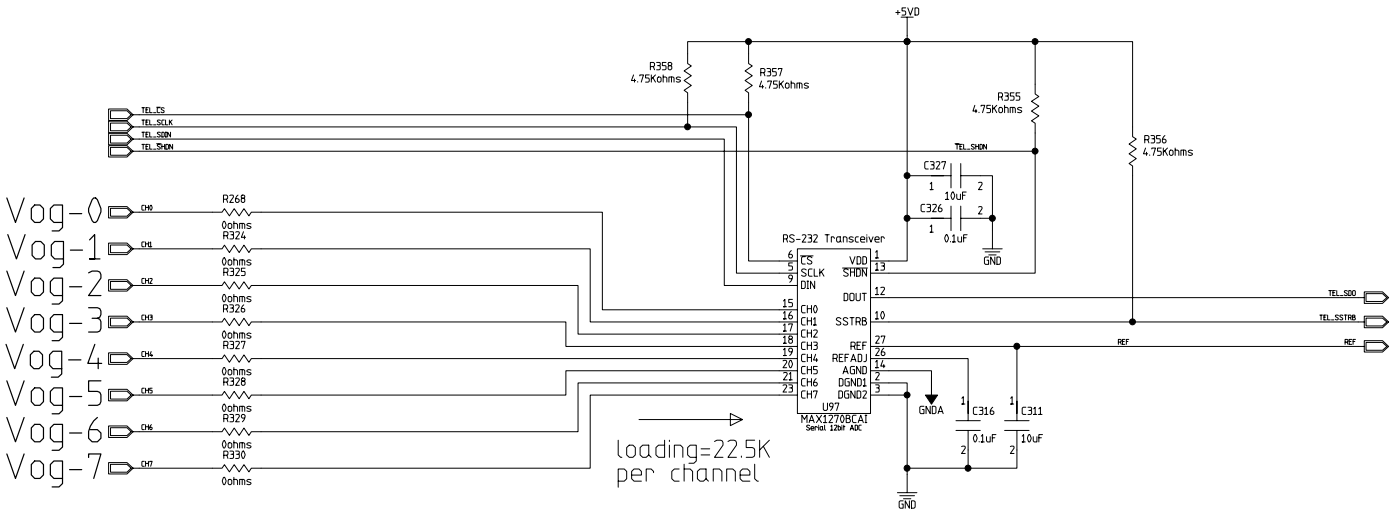
MODIFIED 12/7/2007 9:04:47 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

Telemetry ADC 40-47

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D



TELEMETRY CHANNELS BIAS 32-39
READ Memory Location 0x460-467

MODFIED 12/7/2007 9:04:20 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

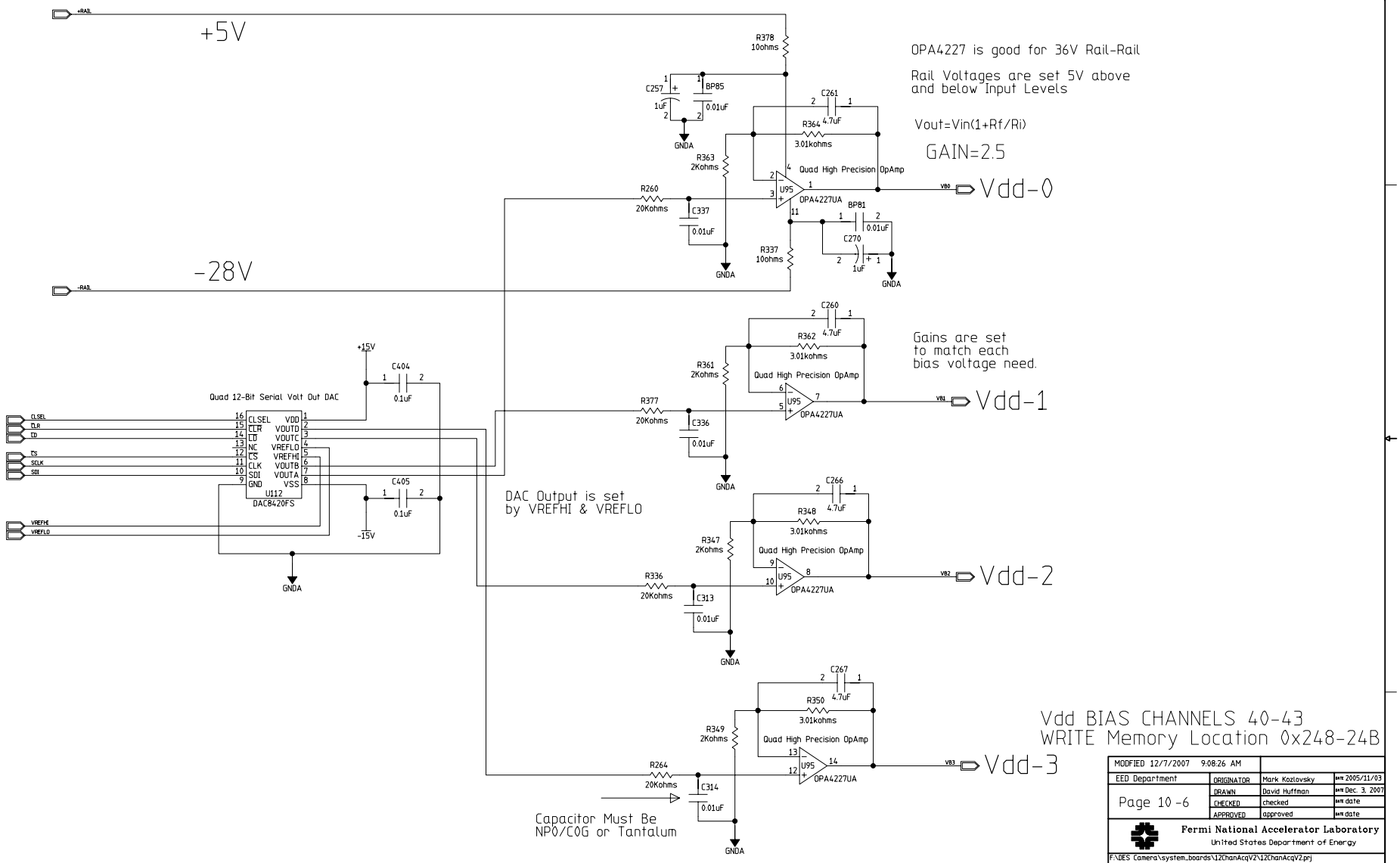
Fermi National Accelerator Laboratory
United States Department of Energy

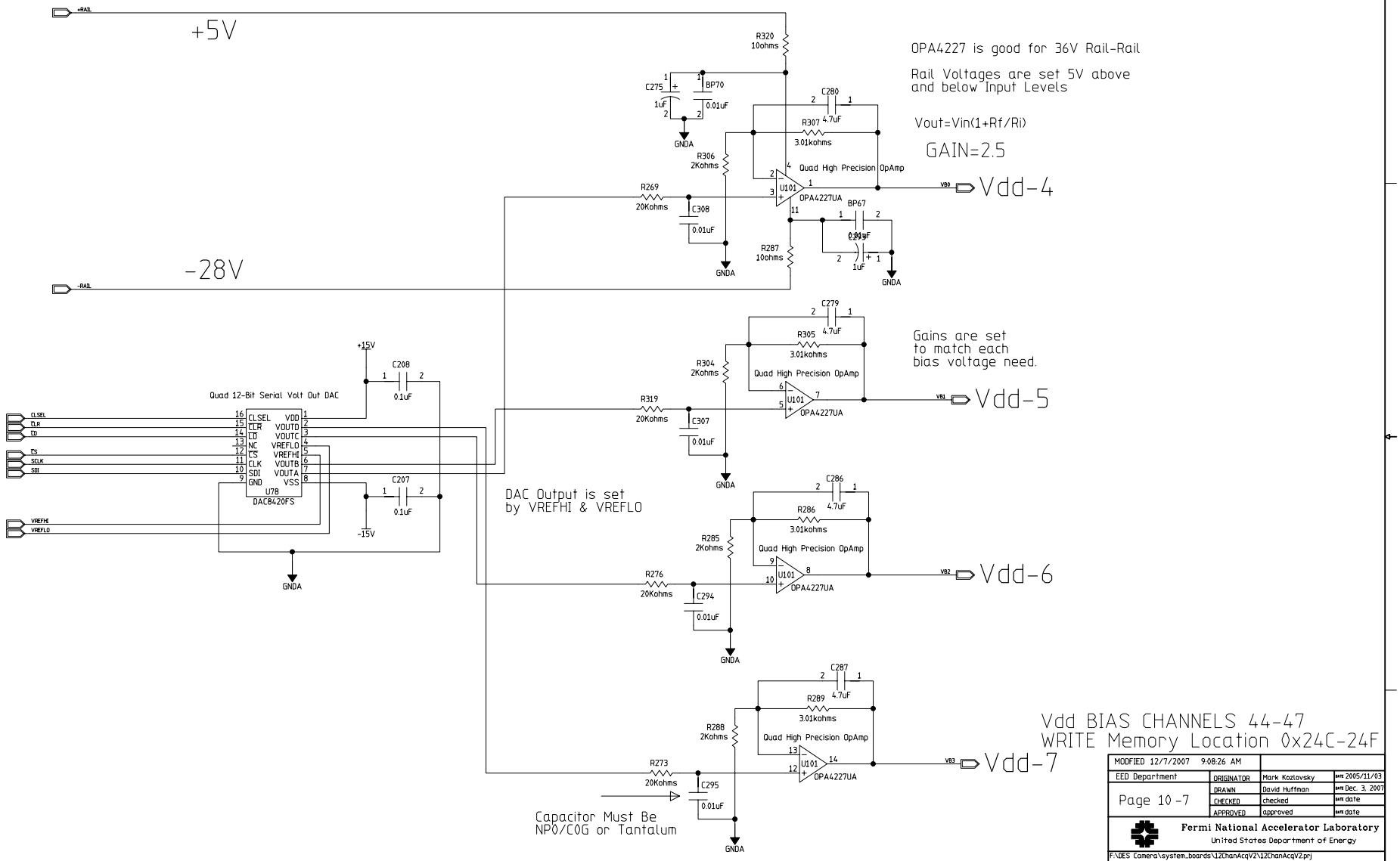
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

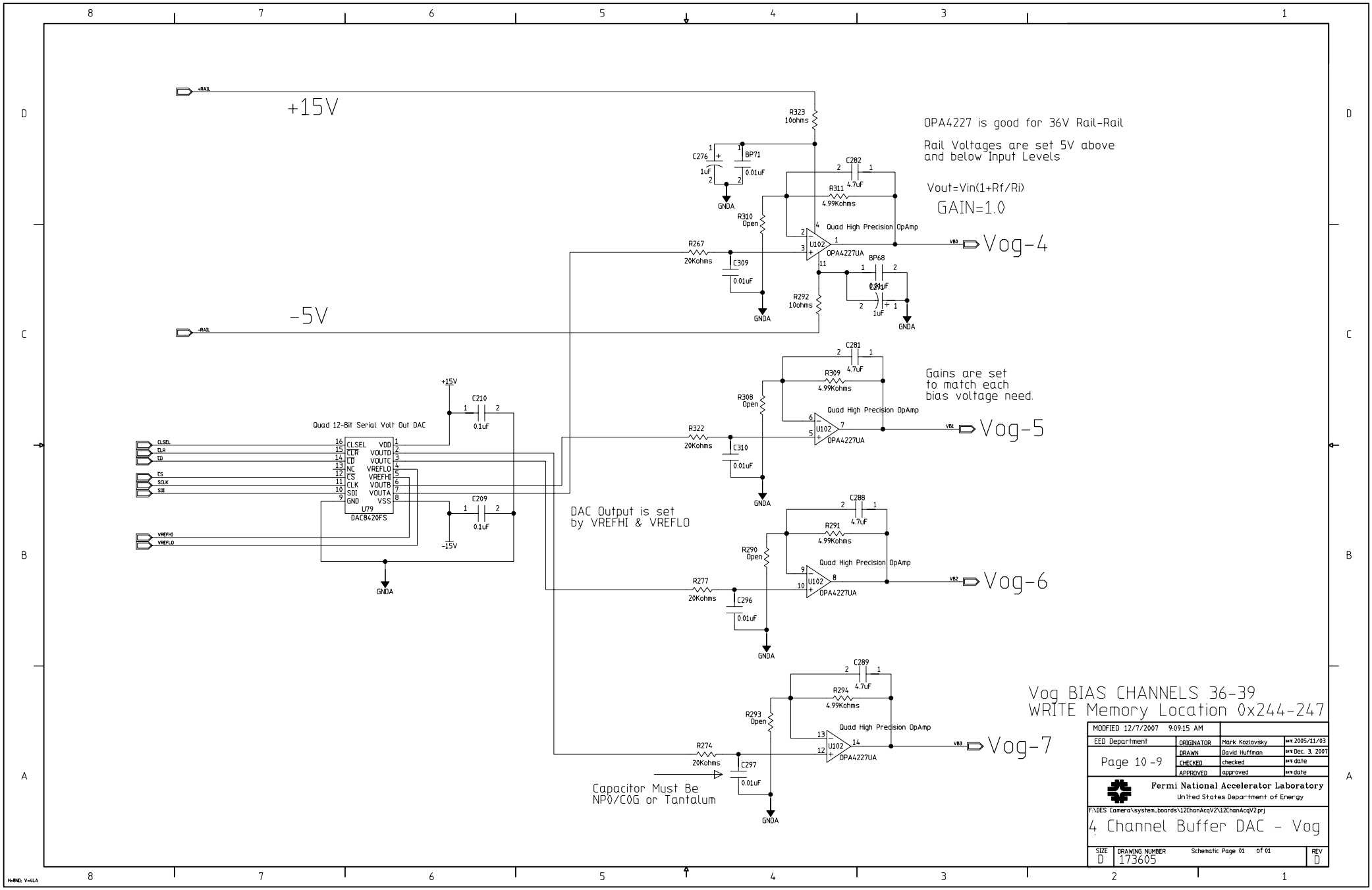
.Telemetry ADC 32-39

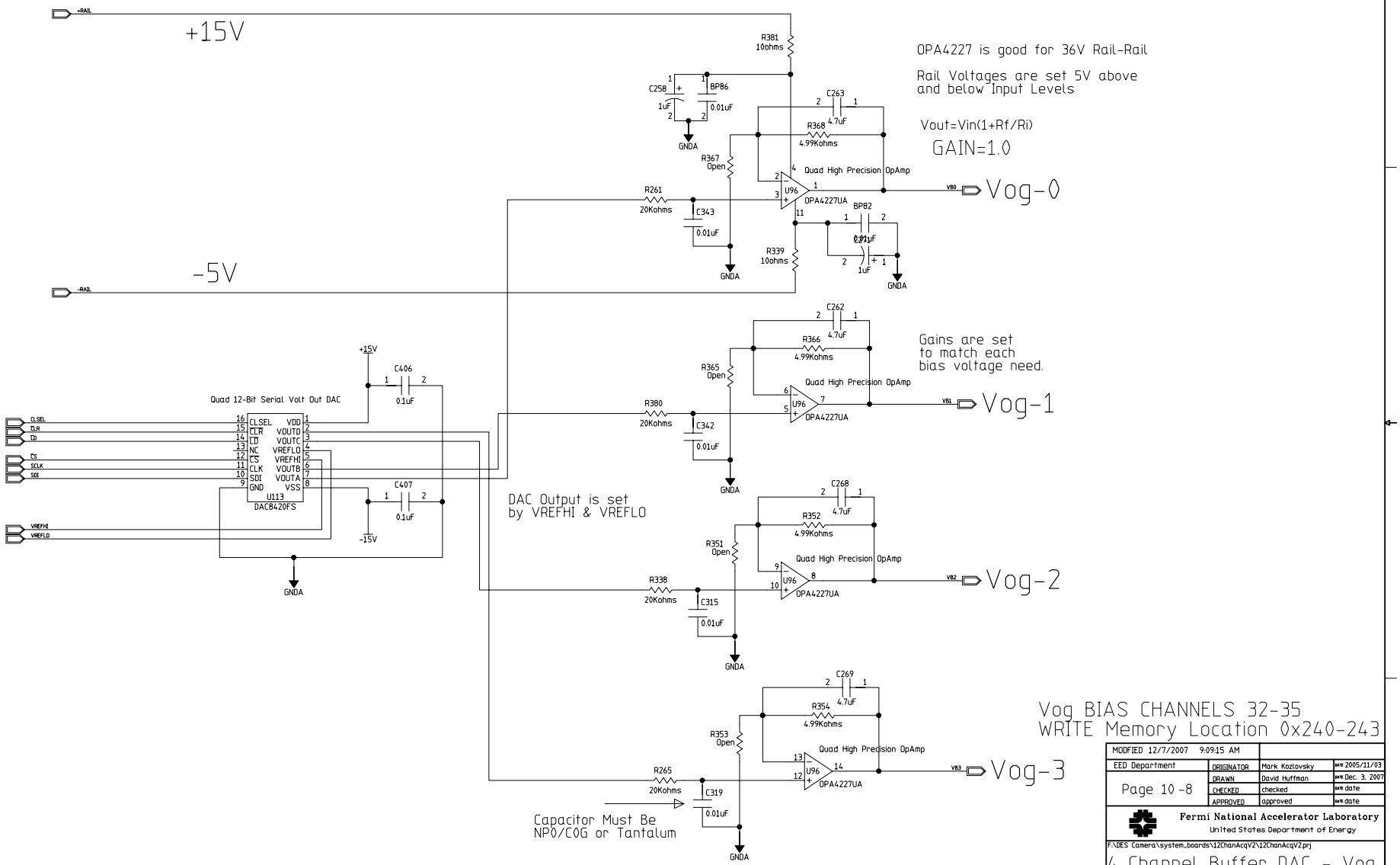
SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 Of 01	D

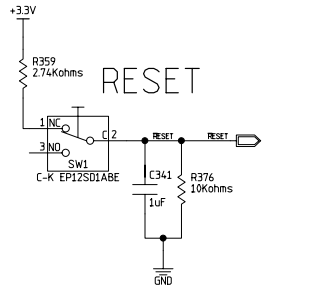
H=BND: V=4LA

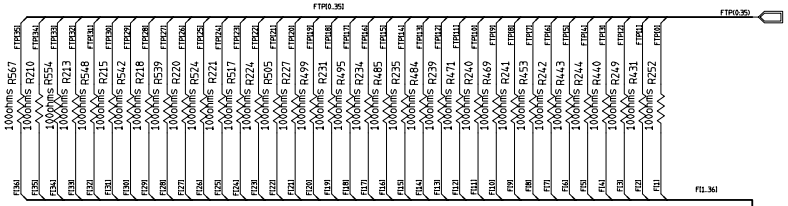

+5V
-28V
+RAIL
-RAIL
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=2.5
Quad High Precision OpAmp
OPA4227UA
Vdd-0
Vdd-1
Vdd-2
Vdd-3
Gains are set to match each bias voltage need.
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
DAC Output is set by VREFHI & VREFLO
Capacitor Must Be NP0/C0G or Tantalum
GNDA
Vdd BIAS CHANNELS 40-43
WRITE Memory Location 0x248-24B
MODIFIED 12/7/2007 9:08:26 AM
EED Department
Page 10 -6
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffered DAC - VDD
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


+RAIL
+5V
-RAIL
-28V
R320
10ohms
C275
1uF
BP70
0.01uF
GNDA
C280
4.7uF
R307
3.01kohms
R306
2Kohms
Quad High Precision OpAmp
U101
OPA4227UA
R269
20Kohms
C308
0.01uF
VB0
Vdd-4
BP67
R287
10ohms
1uF
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=2.5
Gains are set
to match each
bias voltage need.
C279
4.7uF
R305
3.01kohms
R304
2Kohms
R319
20Kohms
C307
0.01uF
VB1
Vdd-5
+15V
C208
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
CD
CS
SCLK
SDI
VREFHI
VREFLO
U78
DAC8420FS
C207
-15V
DAC Output is set
by VREFHI & VREFLO
C286
4.7uF
R286
3.01kohms
R285
2Kohms
R276
20Kohms
C294
0.01uF
VB2
Vdd-6
C287
4.7uF
R289
3.01kohms
R288
2Kohms
R273
20Kohms
C295
0.01uF
VB3
Vdd-7
Capacitor Must Be
NP0/C0G or Tantalum
Vdd BIAS CHANNELS 44-47
WRITE Memory Location 0x24C-24F
MODIFIED 12/7/2007 9:08:26 AM
EED Department
Page 10 -7
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffered DAC - VDD
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

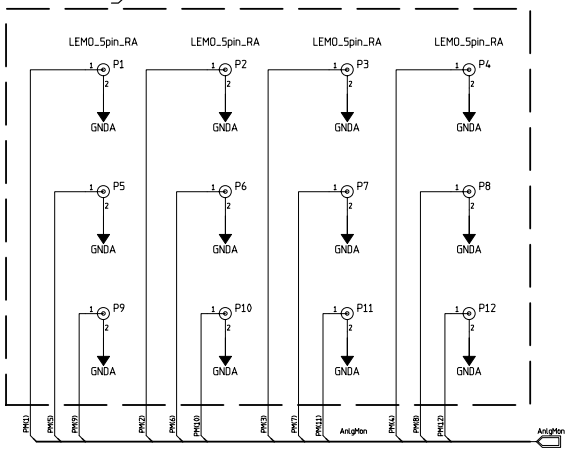

+RAIL
+15V
-RAIL
-5V
R323
10ohms
C276
1uF
BP71
0.01uF
GNDA
C282
4.7uF
R311
4.99Kohms
R310
Open
Quad High Precision OpAmp
U102
OPA4227UA
R267
20Kohms
C309
0.01uF
BP68
0.01uF
1uF
R292
10ohms
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.0
VB0
Vog-4
C281
4.7uF
R309
4.99Kohms
R308
Open
R322
20Kohms
C310
0.01uF
Gains are set
to match each
bias voltage need.
VB1
Vog-5
C288
4.7uF
R291
4.99Kohms
R290
Open
R277
20Kohms
C296
0.01uF
VB2
Vog-6
C289
4.7uF
R294
4.99Kohms
R293
Open
R274
20Kohms
C297
0.01uF
VB3
Vog-7
+15V
C210
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
TLR
TD
CS
SCLK
SDI
VREFHI
VREFLO
CLSEL
CLR
TD
NC
CS
CLK
SDI
GND
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
U79
DAC8420FS
C209
0.1uF
-15V
GNDA
DAC Output is set
by VREFHI & VREFLO
Capacitor Must Be
NP0/C0G or Tantalum
Vog BIAS CHANNELS 36-39
WRITE Memory Location 0x244-247
MODFIED 12/7/2007 9:09:15 AM
EED Department
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Page 10-9
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffer DAC - Vog
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D


+15V
-5V
+RAIL
-RAIL
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.0
Gains are set to match each bias voltage need.
DAC Output is set by VREFHI & VREFLO
Capacitor Must Be NP0/C0G or Tantalum
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
Quad High Precision OpAmp
OPA4227UA
Vog-0
Vog-1
Vog-2
Vog-3
GNDA
Vog BIAS CHANNELS 32-35
WRITE Memory Location 0x240-243
MODFIED 12/7/2007 9:09:15 AM
EED Department
Page 10-8
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Dec. 3, 2007
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj
4 Channel Buffer DAC - Vog
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV D

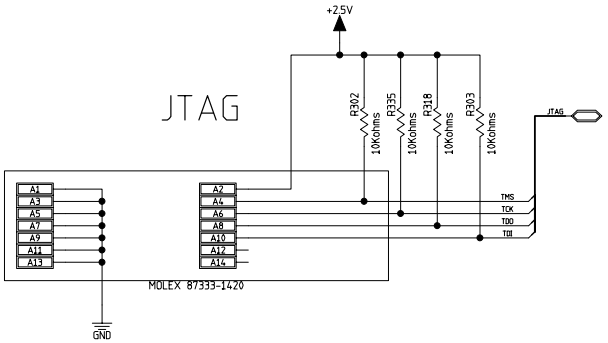




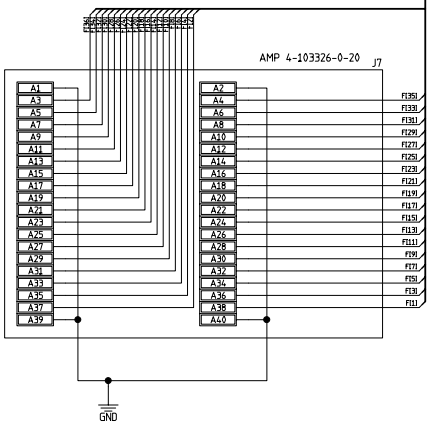
Analog Test Points



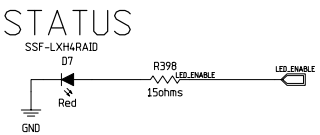
JTAG



Digital Test Points



STATUS



MODFIED 12/3/2007 2:52:34 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 14	DRAWN	David Huffman	DATE Dec. 3, 2007
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

F:\DES Camera\system_boards\12ChanAcqV2\12ChanAcqV2.prj

J6 Test Points/ Analog Mon
J7 JTAG

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	D

H=BND: V=4LA