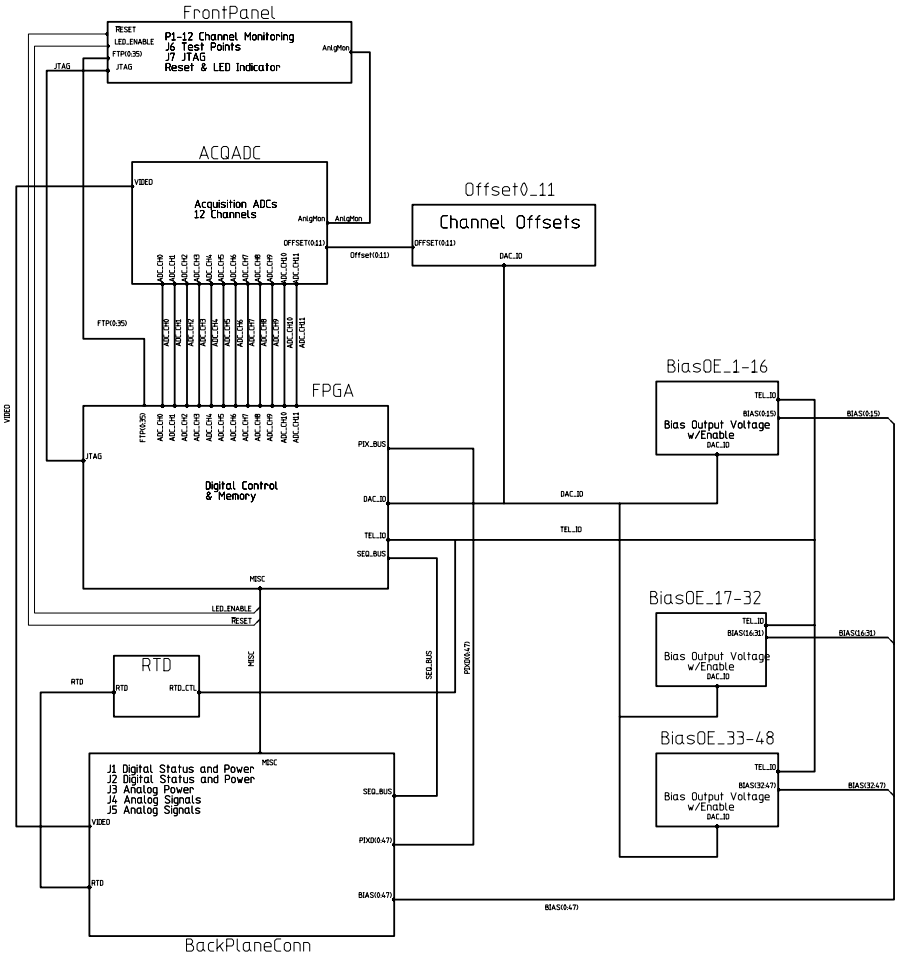

MODFIED 10/25/2006 3:32:00 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 1	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
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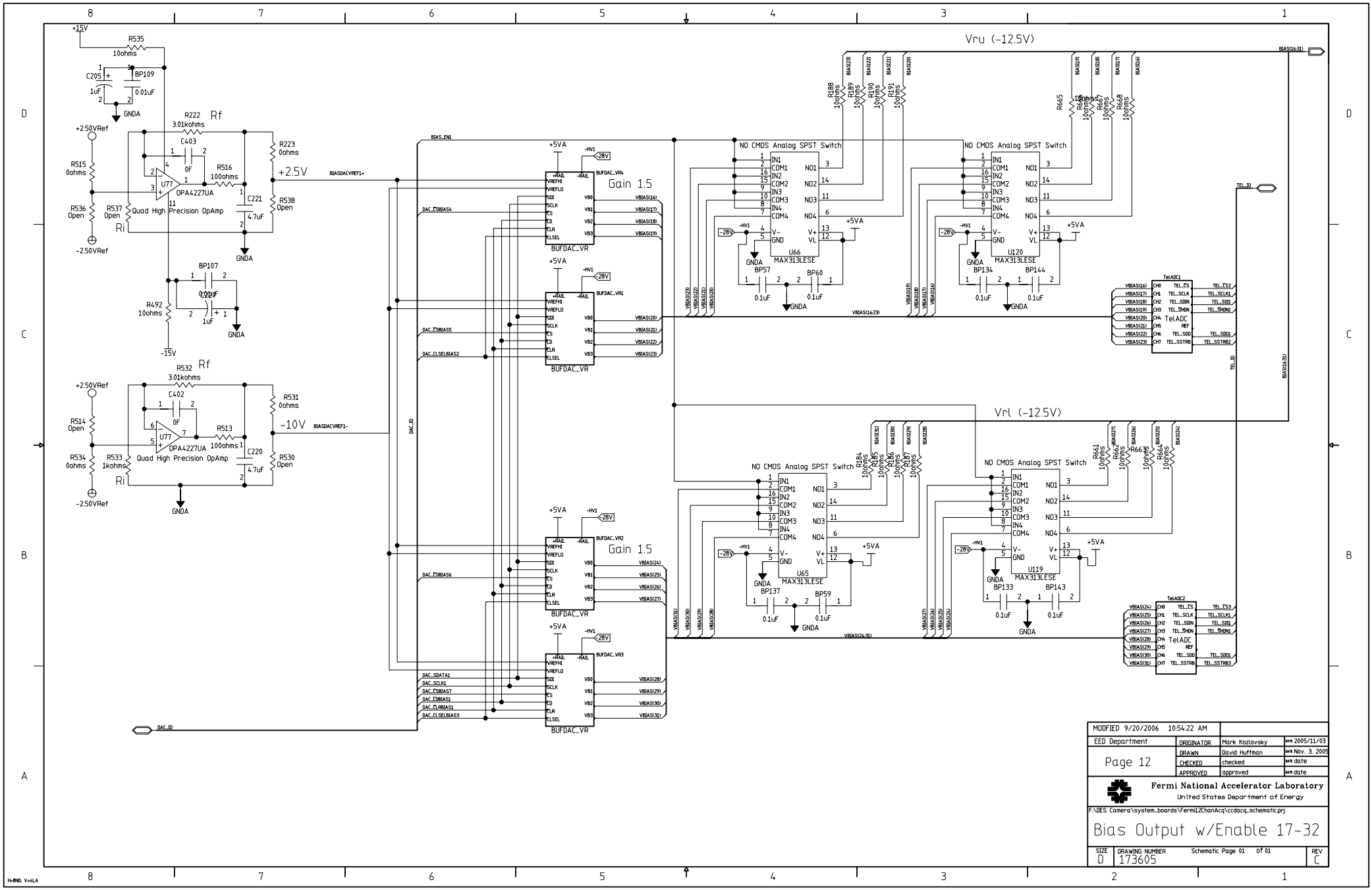
ACQUISITION BOARD
TOP LEVEL

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		C

H=BND: V=4LA



MODIFIED 9/20/2006 10:54:22 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 12	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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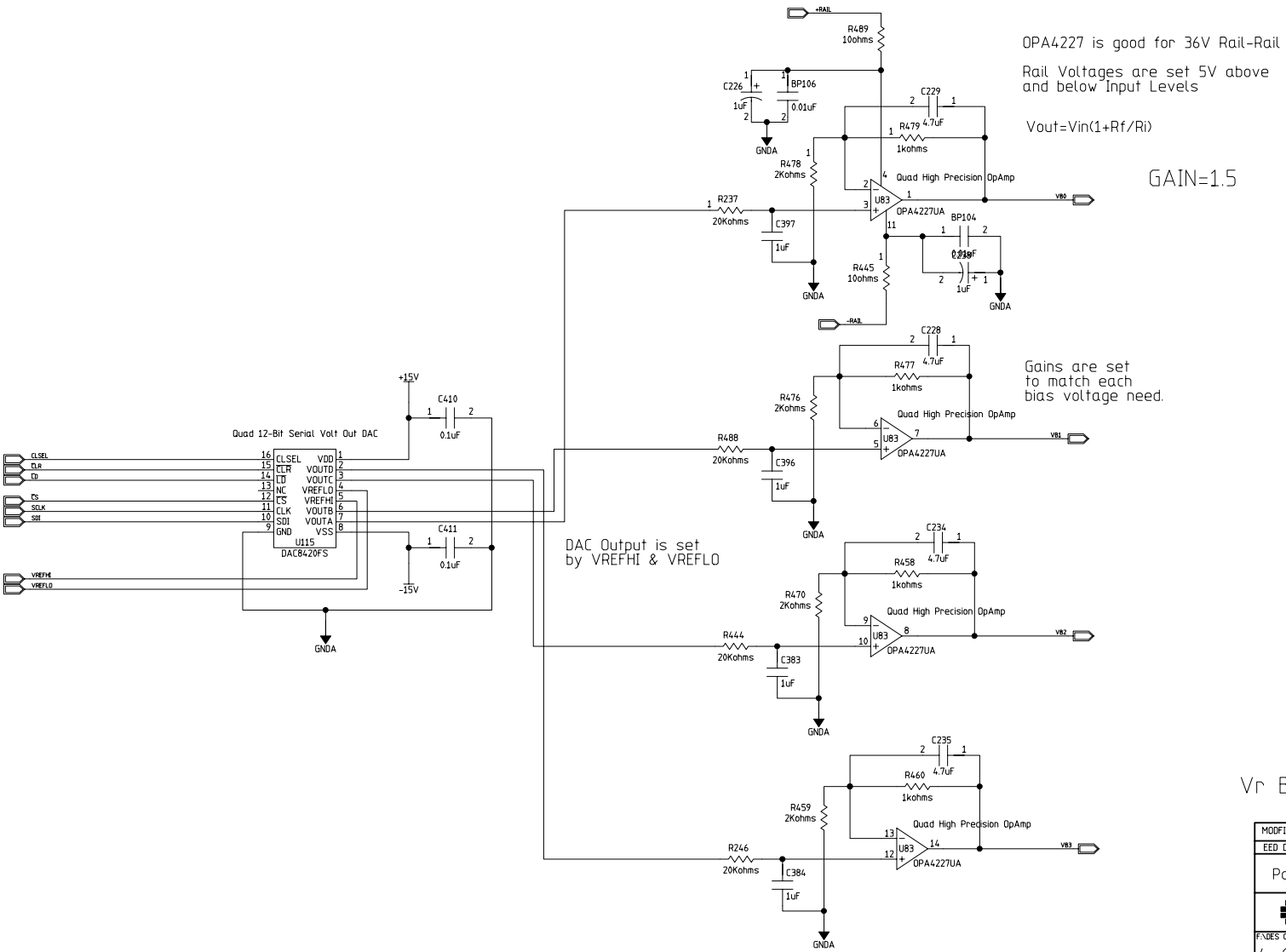
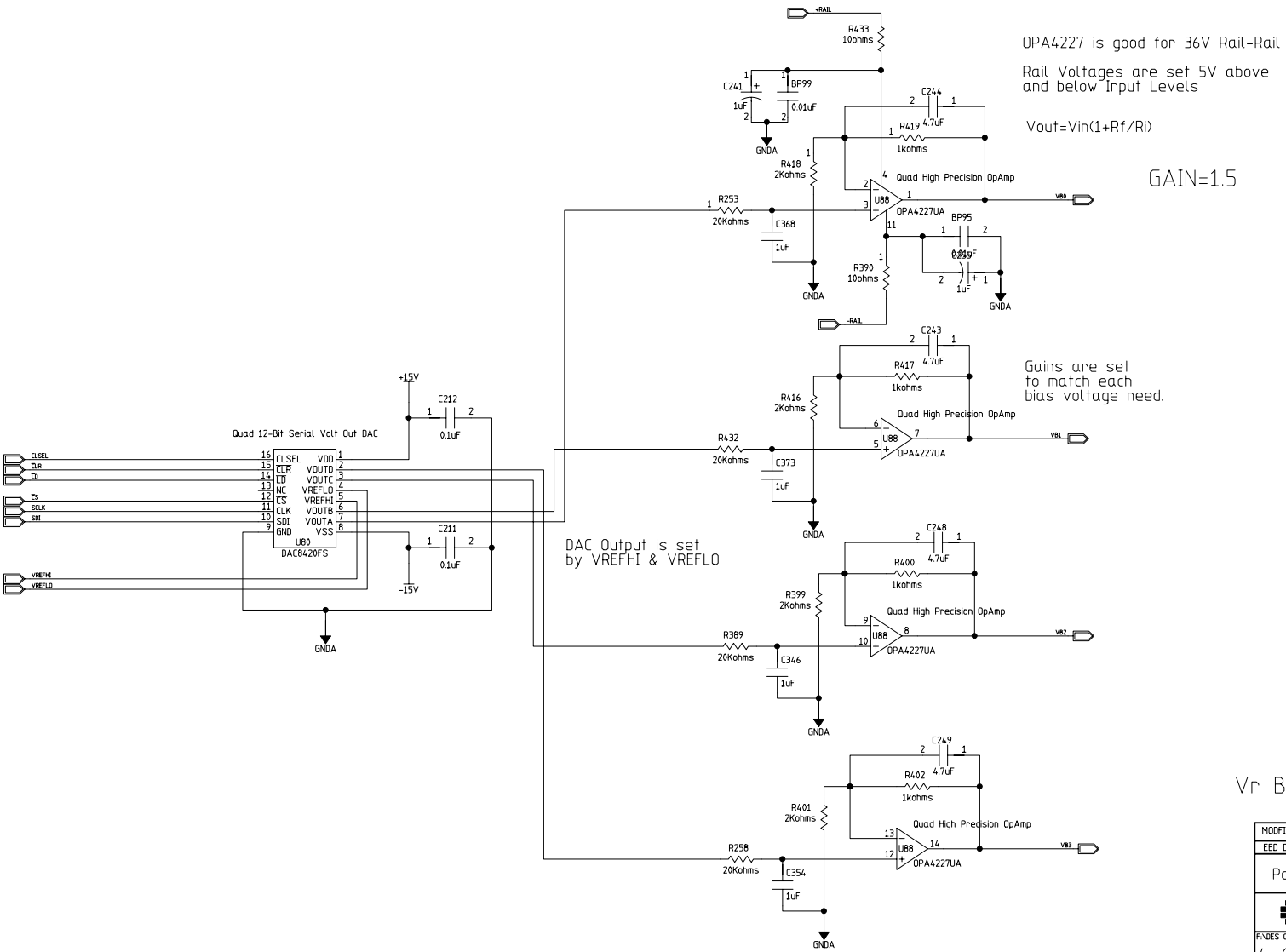
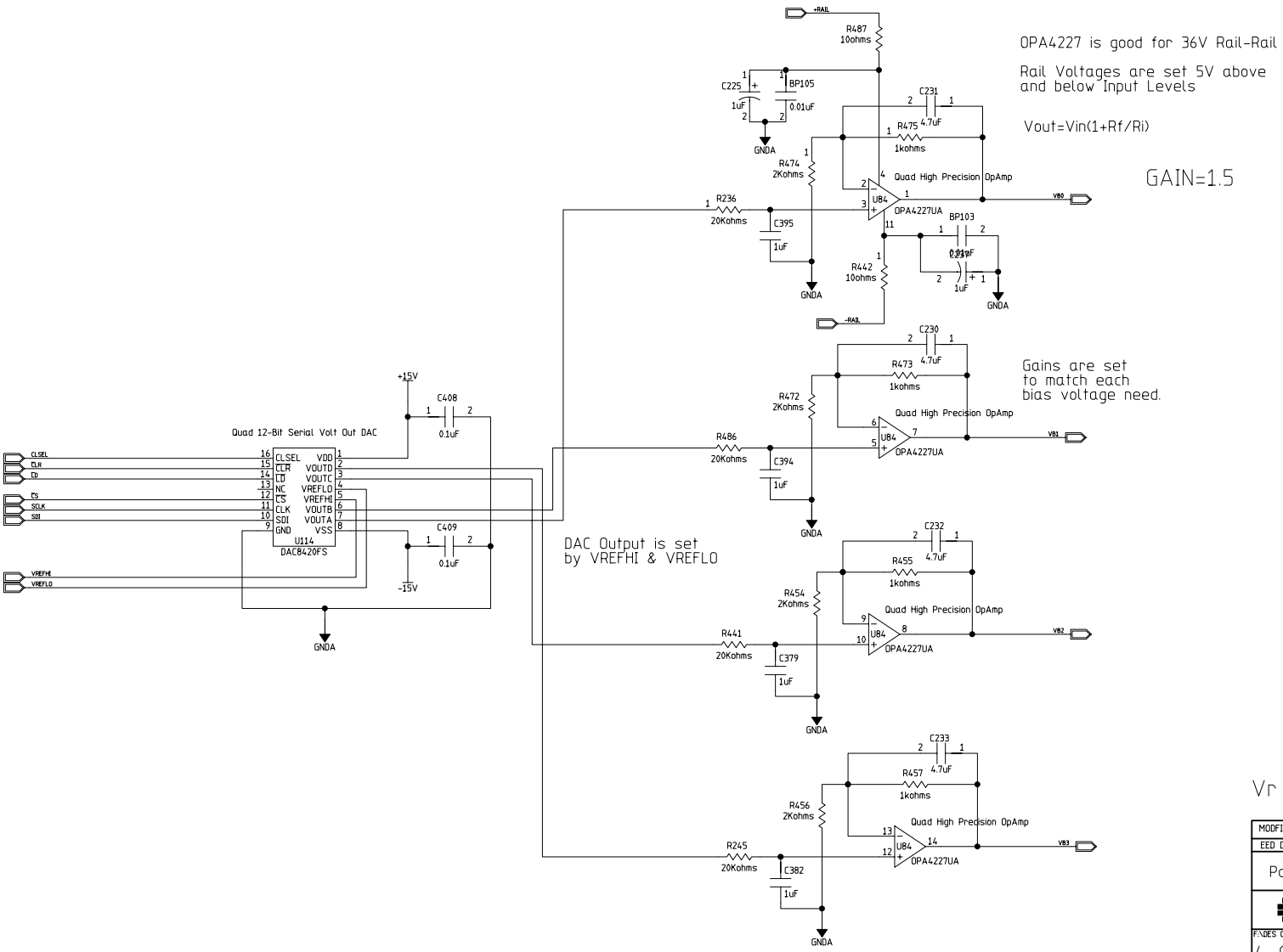
Bias Output w/Enable 17-32

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		C


+RAIL
R489
10ohms
C226
1uF
BP106
0.01uF
GNDA
C229
4.7uF
R479
1kohms
R478
2Kohms
Quad High Precision OpAmp
U83
OPA4227UA
VB0
R237
20Kohms
C397
1uF
BP104
R445
10ohms
-RAIL
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
C228
4.7uF
R477
1kohms
R476
2Kohms
R488
20Kohms
C396
1uF
VB1
Gains are set
to match each
bias voltage need.
+15V
C410
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U115
DAC8420FS
C411
0.1uF
-15V
DAC Output is set
by VREFHI & VREFLO
C234
4.7uF
R458
1kohms
R470
2Kohms
R444
20Kohms
C383
1uF
VB2
C235
4.7uF
R460
1kohms
R459
2Kohms
R246
20Kohms
C384
1uF
VB3
Vr BIAS CHANNELS 16-19
MODIFIED 10/25/2006 10:22:48 AM
EED Department
Page 10 -2
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Nov. 3, 2005
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


+RAIL
R433
10ohms
C241
1uF
BP99
0.01uF
GNDA
C244
4.7uF
R419
1kohms
R418
2Kohms
Quad High Precision OpAmp
U88
OPA4227UA
VB0
R253
20Kohms
C368
1uF
BP95
0.01uF
C357
1uF
R390
10ohms
-RAIL
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
+15V
C212
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U80
DAC8420FS
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
C211
0.1uF
-15V
C243
4.7uF
R417
1kohms
R416
2Kohms
R432
20Kohms
C373
1uF
VB1
Gains are set
to match each
bias voltage need.
DAC Output is set
by VREFHI & VREFLO
C248
4.7uF
R400
1kohms
R399
2Kohms
R389
20Kohms
C346
1uF
VB2
C249
4.7uF
R402
1kohms
R401
2Kohms
R258
20Kohms
C354
1uF
VB3
Vr BIAS CHANNELS 28-31
MODIFIED 10/25/2006 10:22:48 AM
EED Department
Page 10 -5
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Nov. 3, 2005
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



Vr BIAS CHANNELS 24-27

MODIFIED 10/25/2006 10:22:48 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 10-4	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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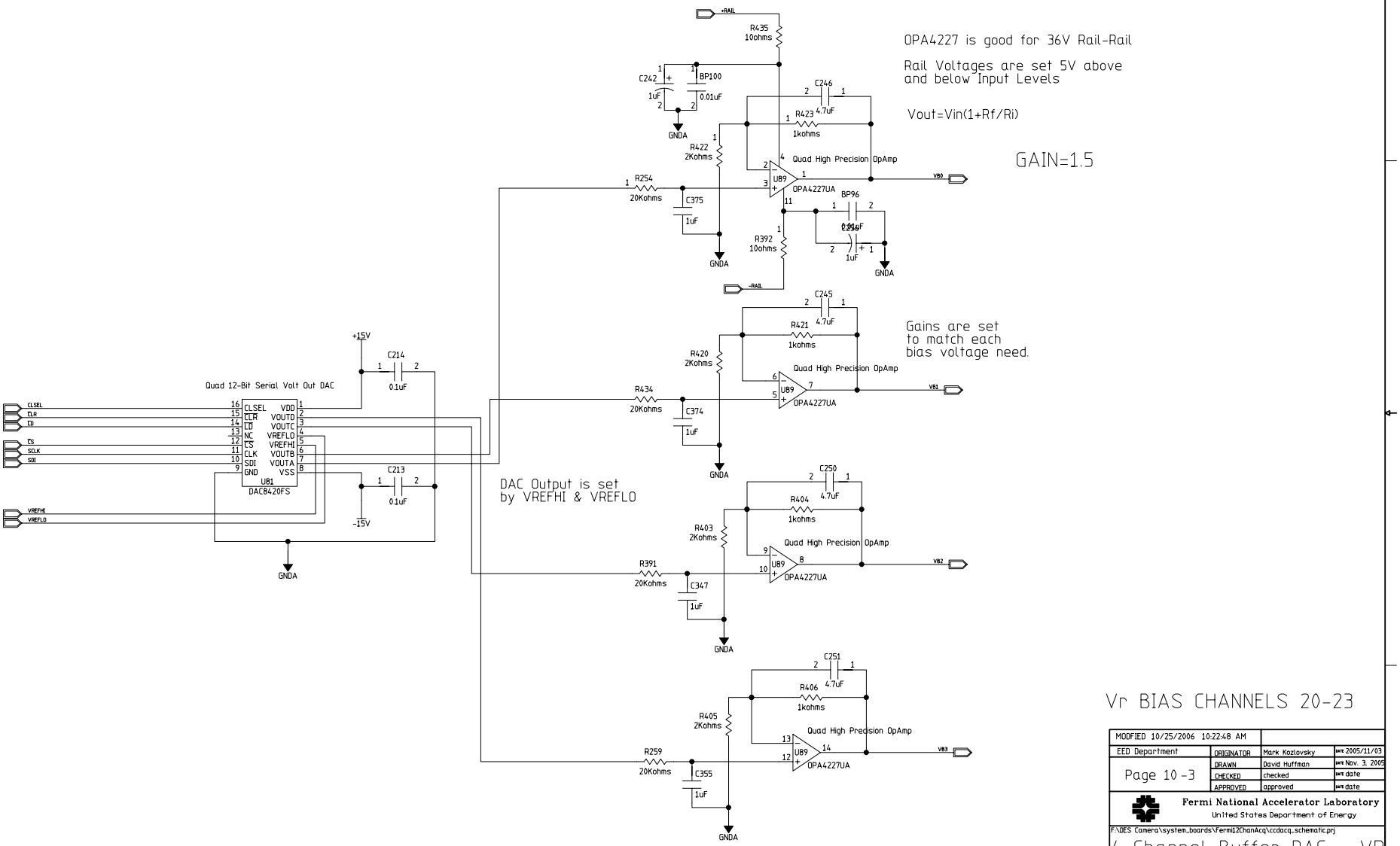
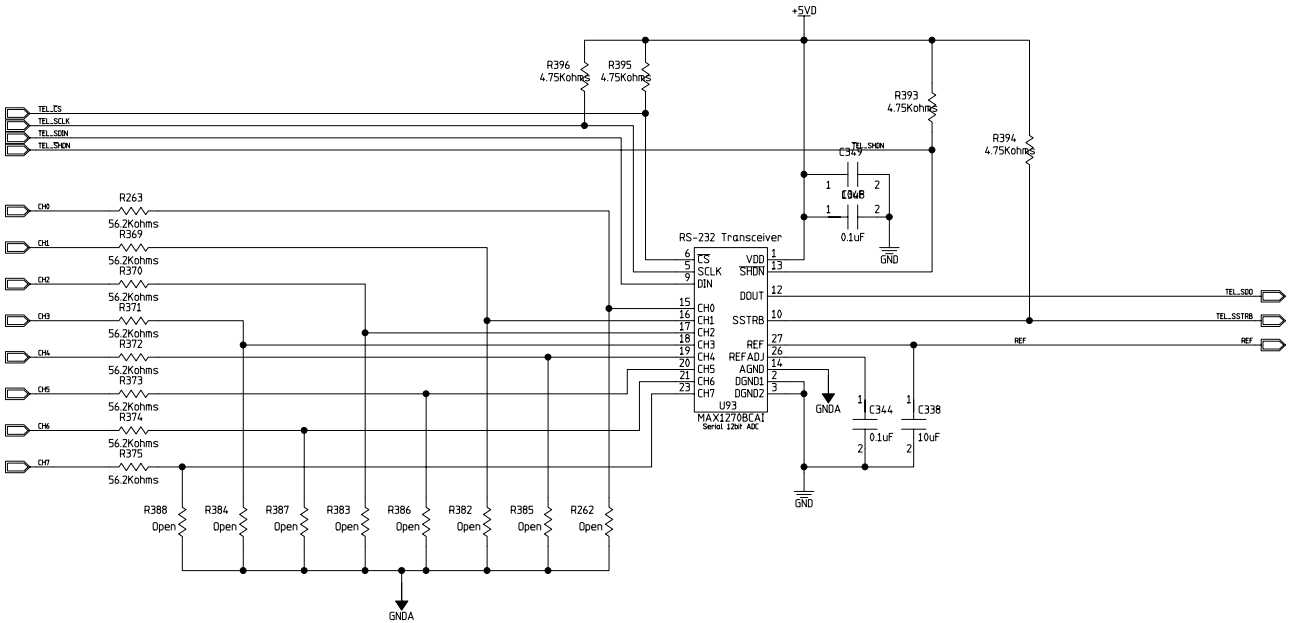
4 Channel Buffer DAC - VR

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C


OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.5
Gains are set to match each bias voltage need.
DAC Output is set by VREFHI & VREFLO
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
Quad High Precision OpAmp
OPA4227UA
+RAIL
-RAIL
+15V
-15V
GNDA
Vr BIAS CHANNELS 20-23
MODIFIED 10/25/2006 10:22:48 AM
EED Department
Page 10-3
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Nov. 3, 2005
CHECKED checked date
APPROVED approved date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
4 Channel Buffer DAC - VR
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



TELEMETRY CHANNELS BIAS 24-31

MODFIED 10/25/2006 3:25:22 PM			
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Page 7-4	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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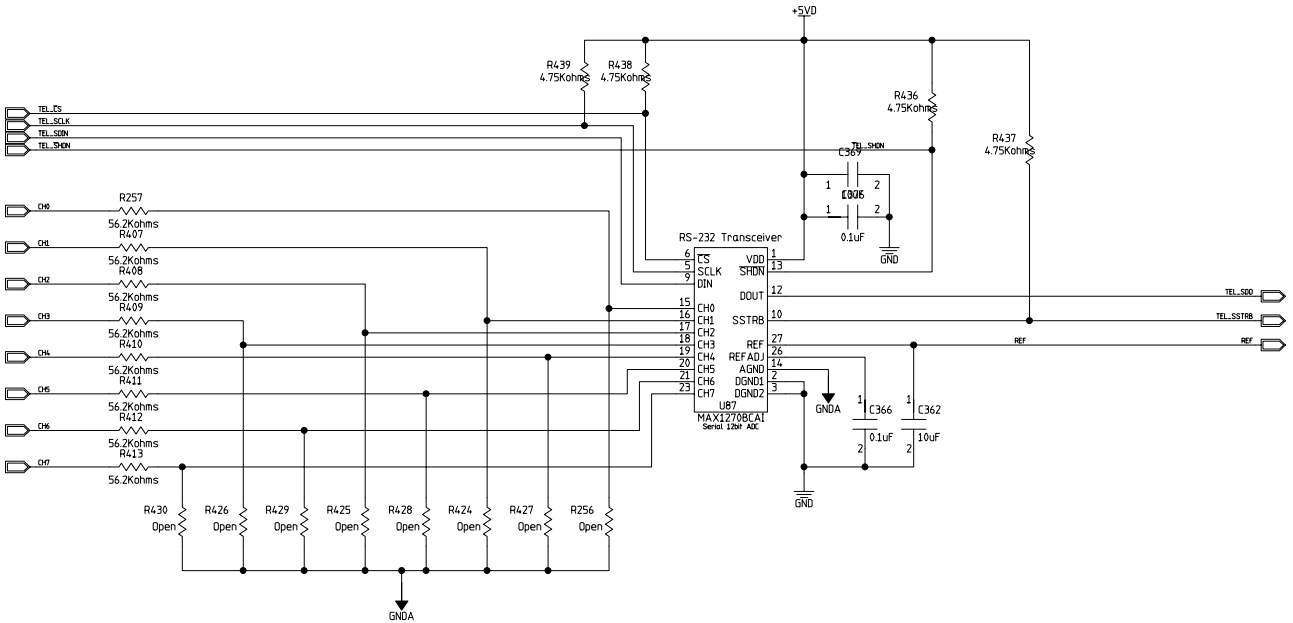
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	Schematic Page 01 Of 01	REV
D	173605		C

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 16-23

MODFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7-3	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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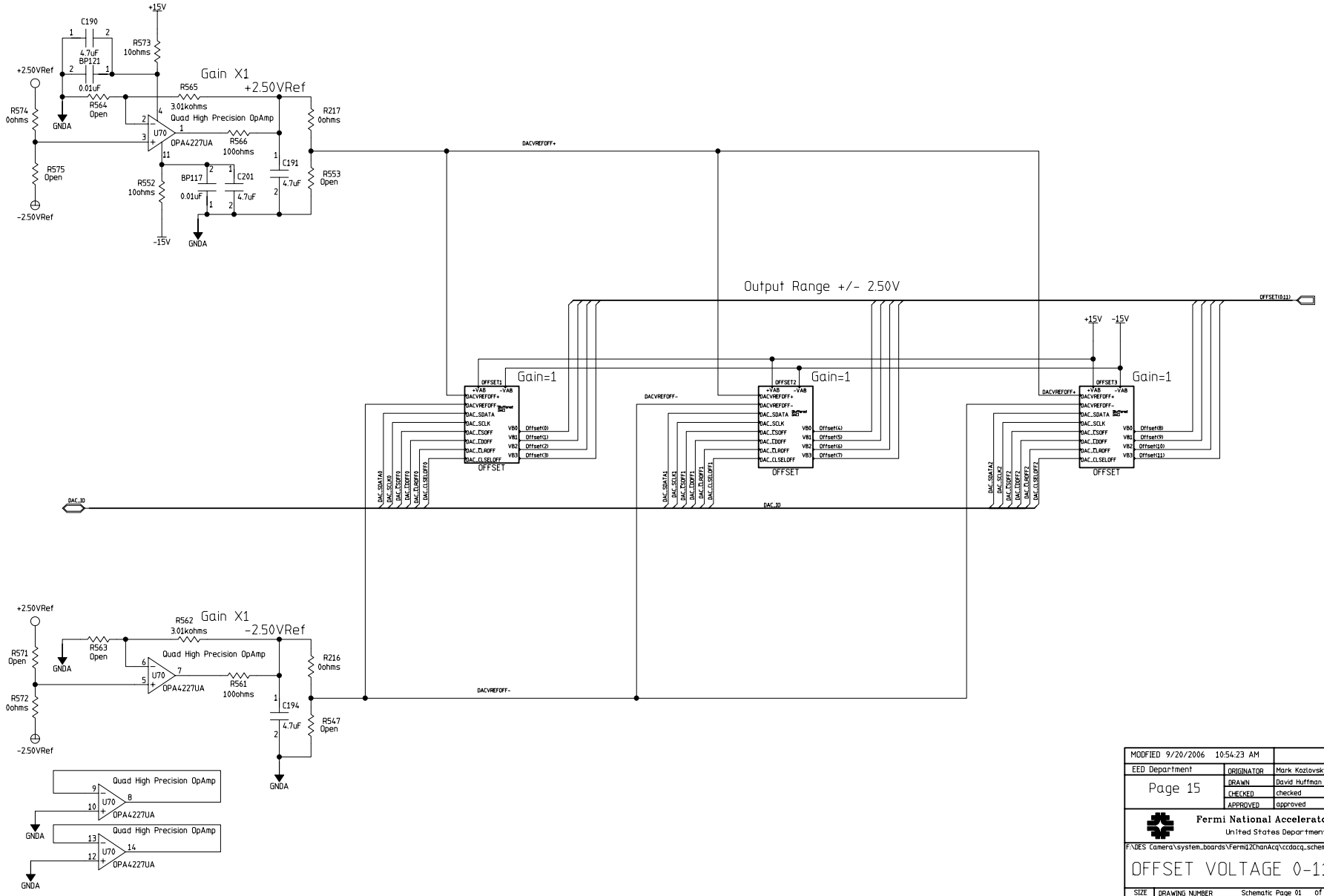
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	Schematic Page 01 Of 01	REV
D	173605		C

H=BND: V=4LA



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 15	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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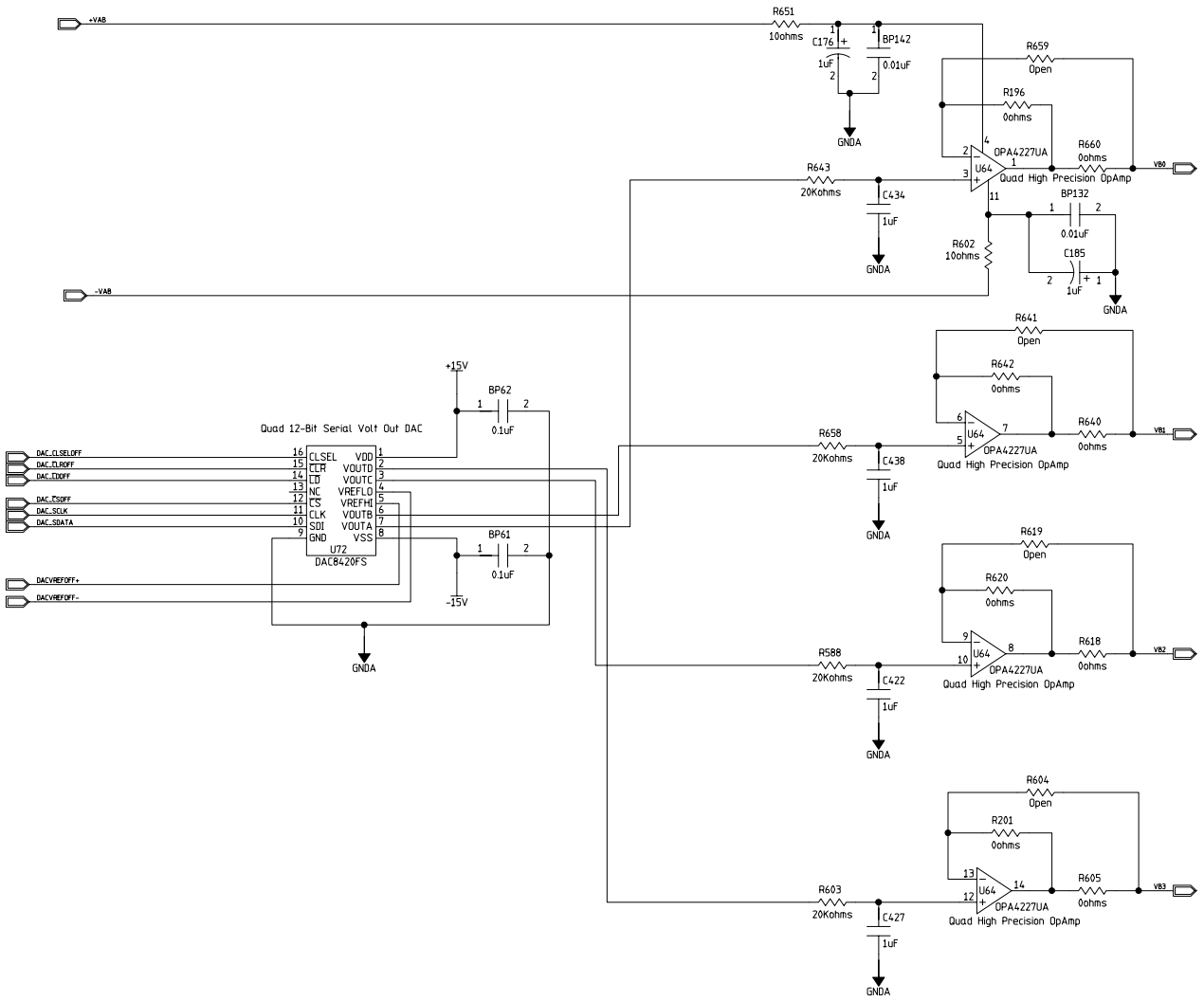
OFFSET VOLTAGE 0-11

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		C



OFFSET DAC CHANNELS 0-3

MODFIED 5/24/2006 12:36:44 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 16 -1	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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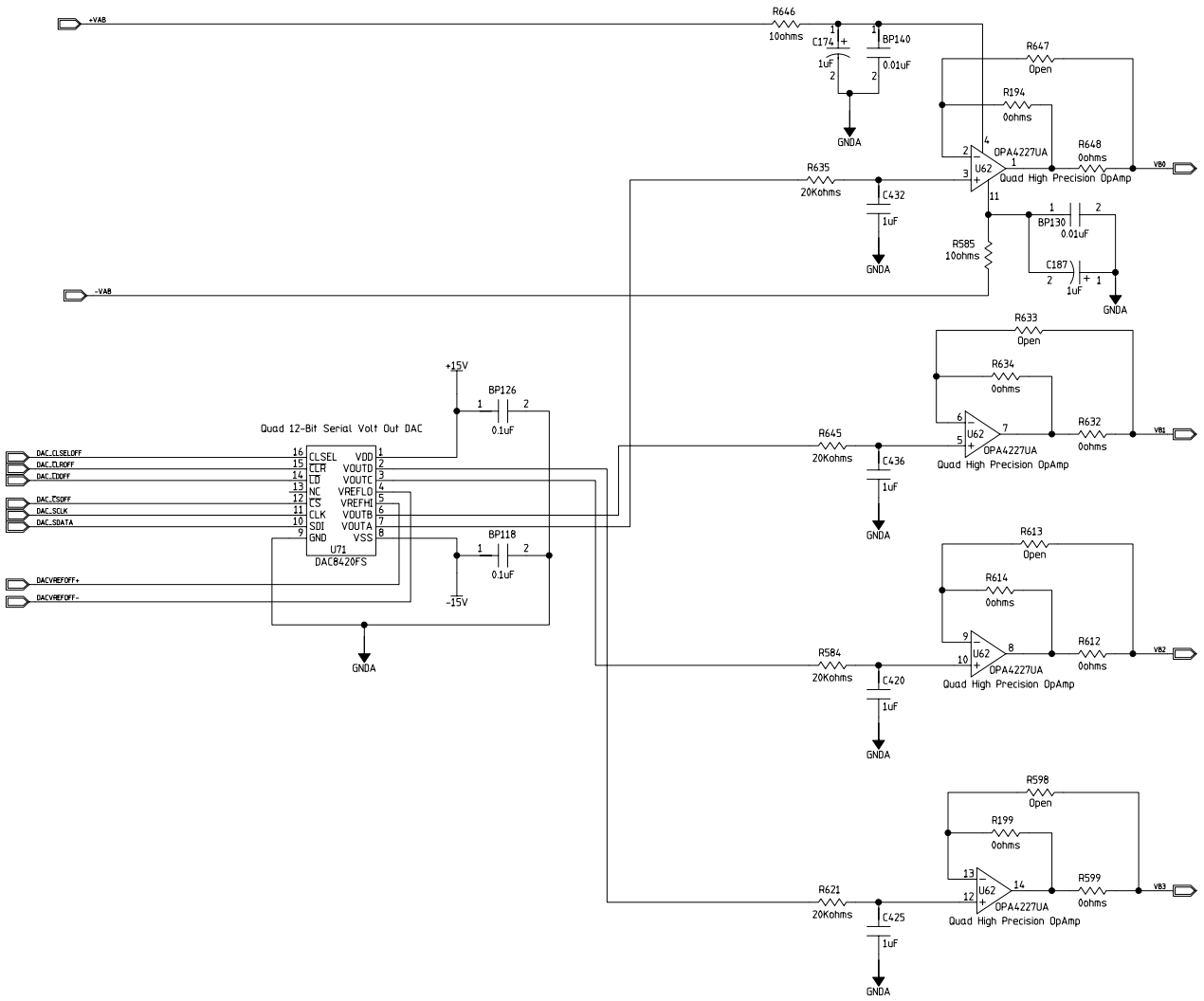
OFFSET DAC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=END: V=4LA



OFFSET DAC CHANNELS 8-11

MODFIED 5/24/2006 12:36:44 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 16-3	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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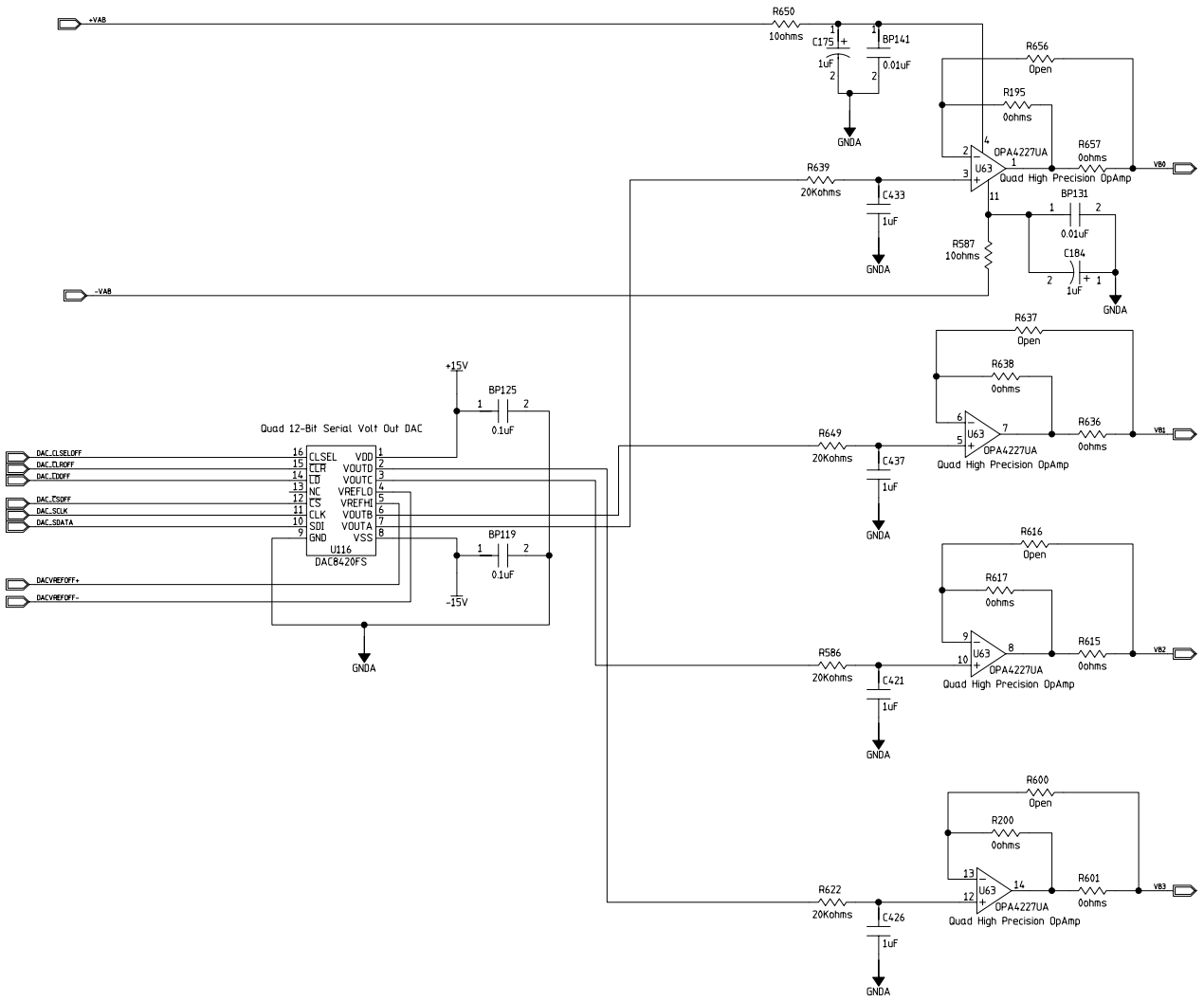
OFFSET DAC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=END: V=4LA



OFFSET DAC CHANNELS 4-7

MODIFIED 5/24/2006 12:36:44 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 16-2	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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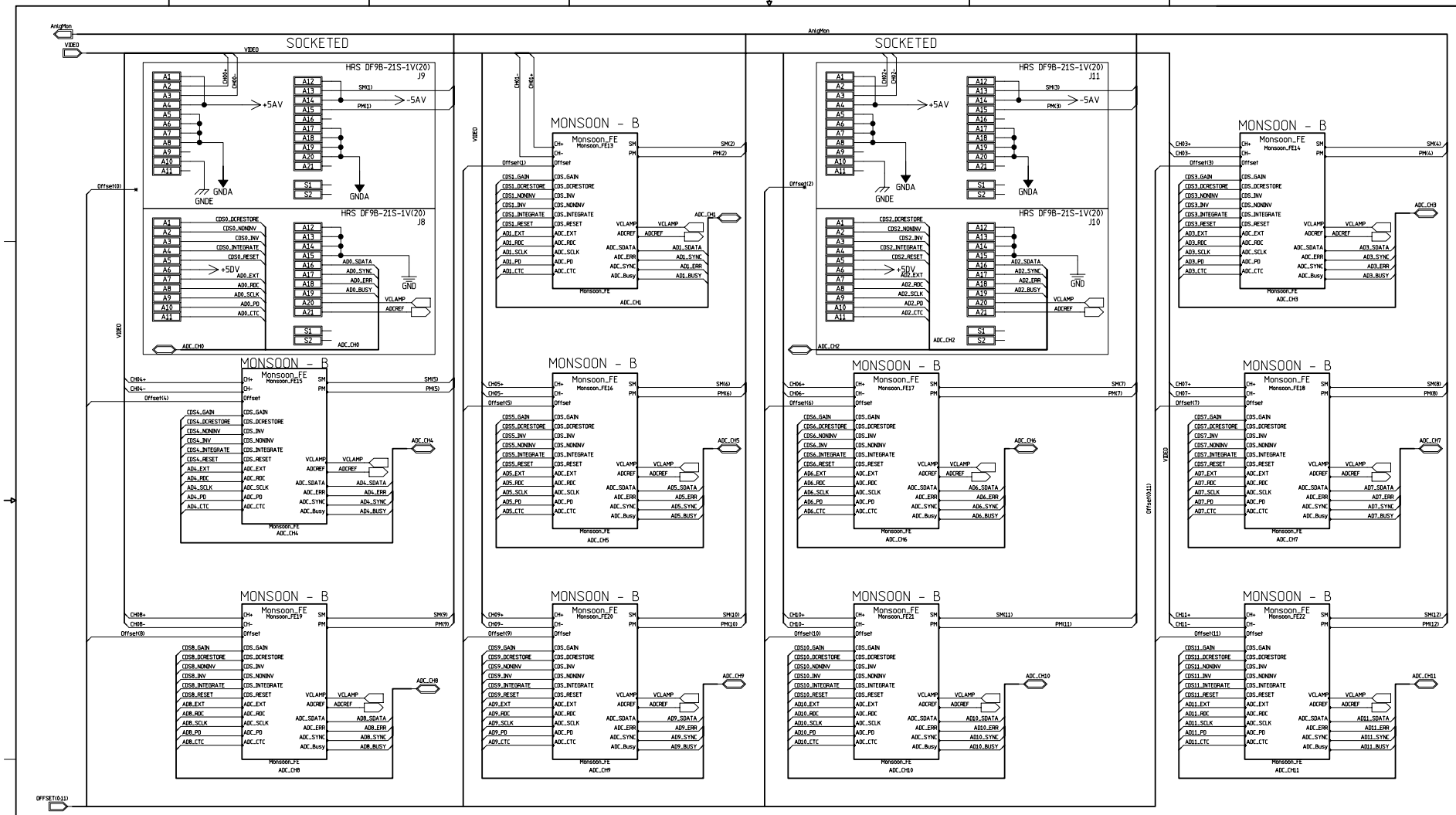
OFFSET DAC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=END: V=4LA



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Page 2	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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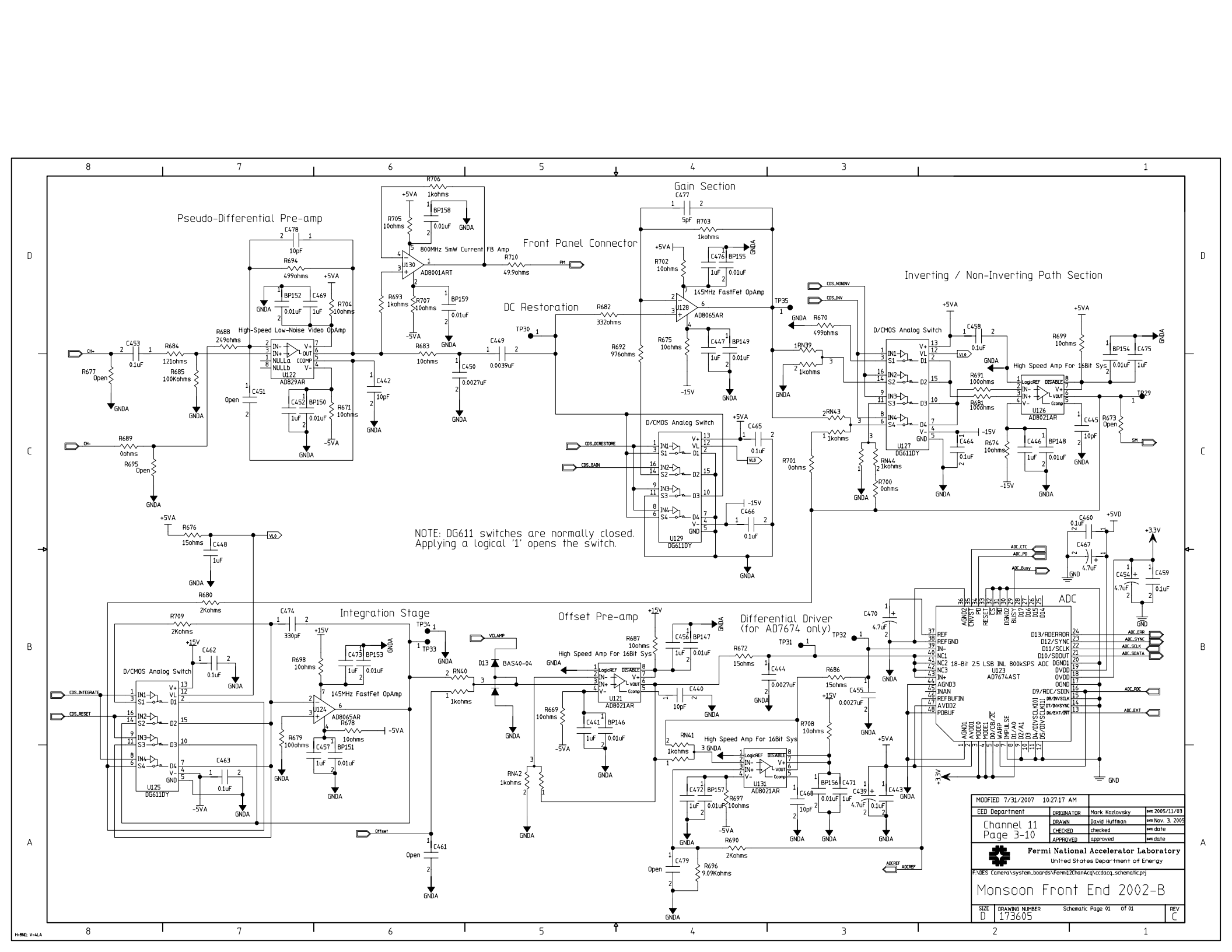
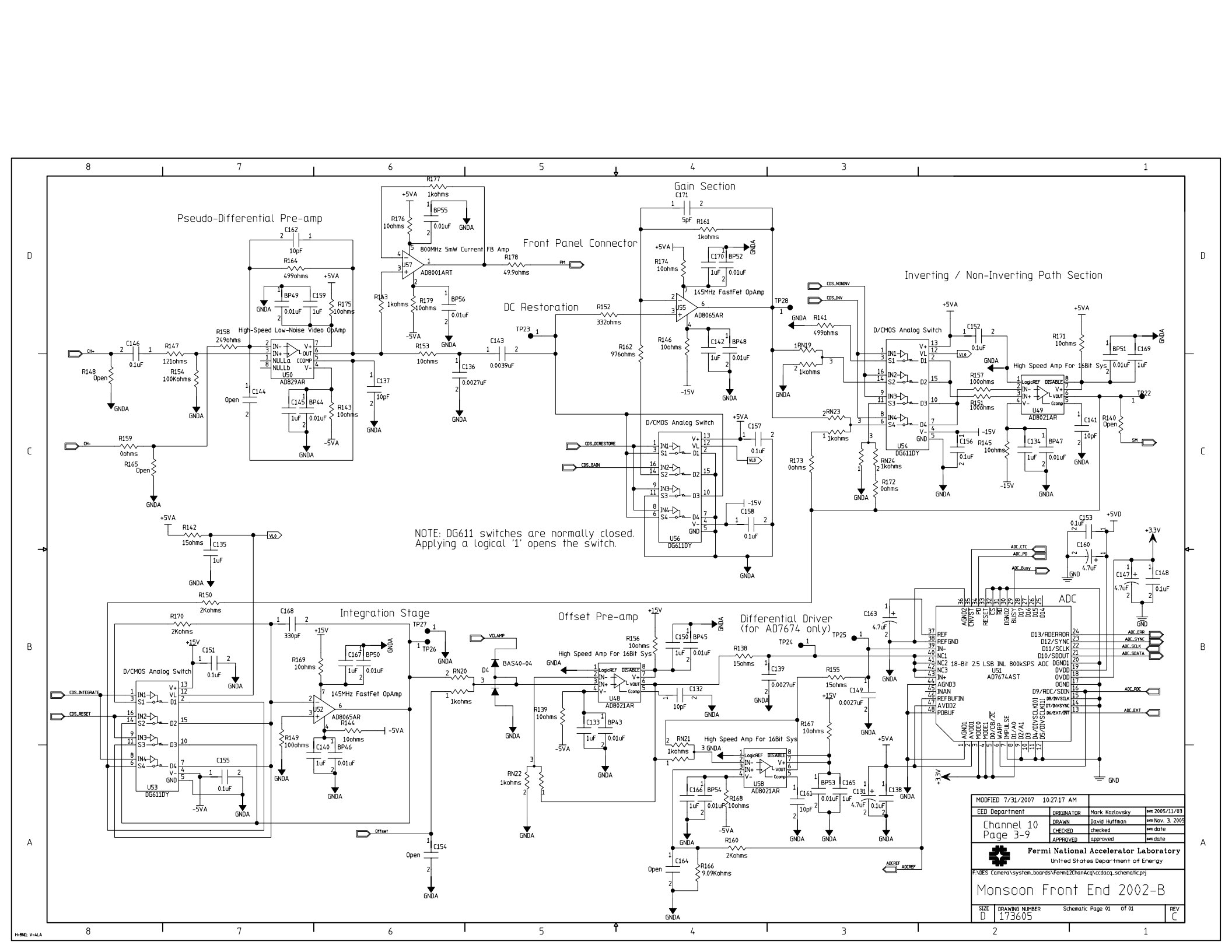
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj

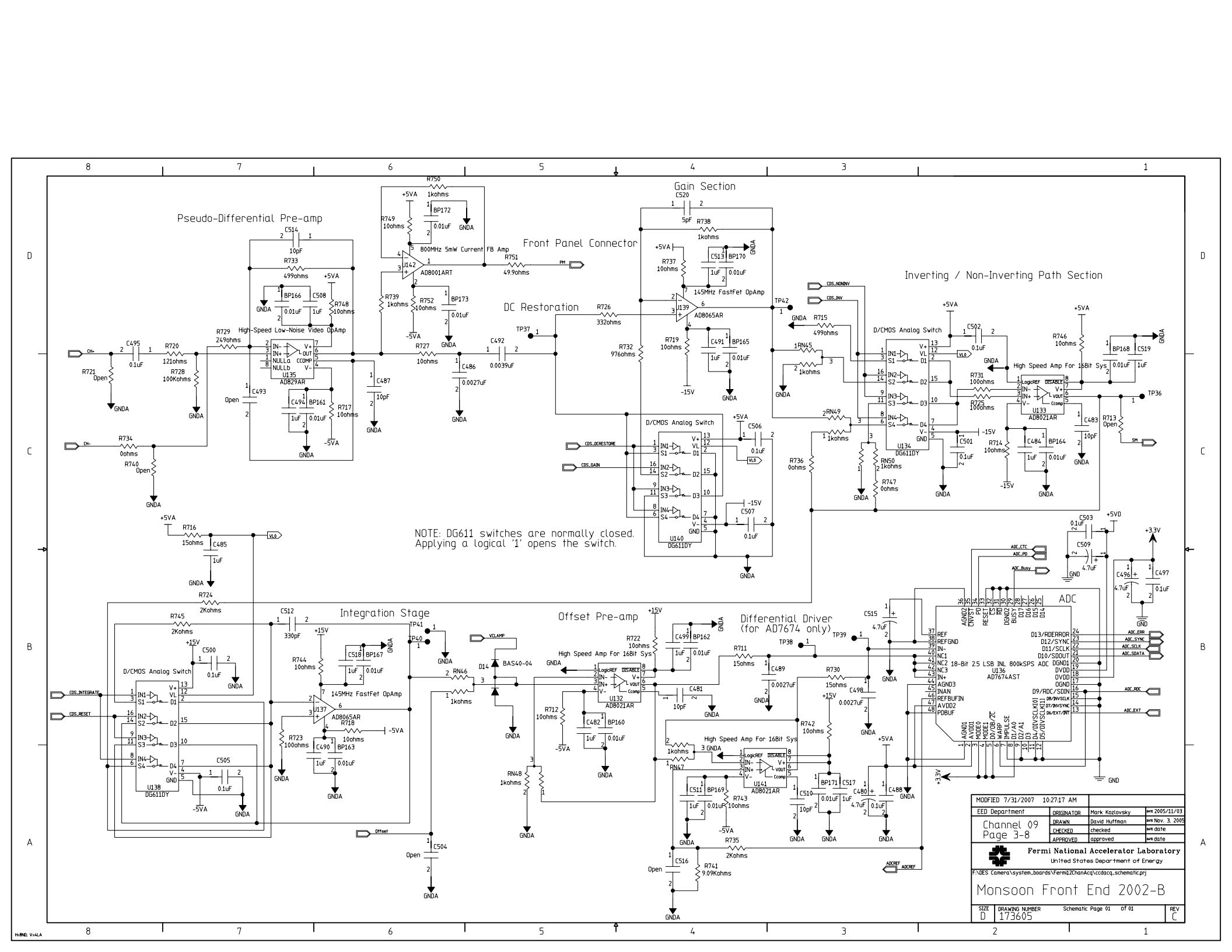
ACQUISITION ADCs

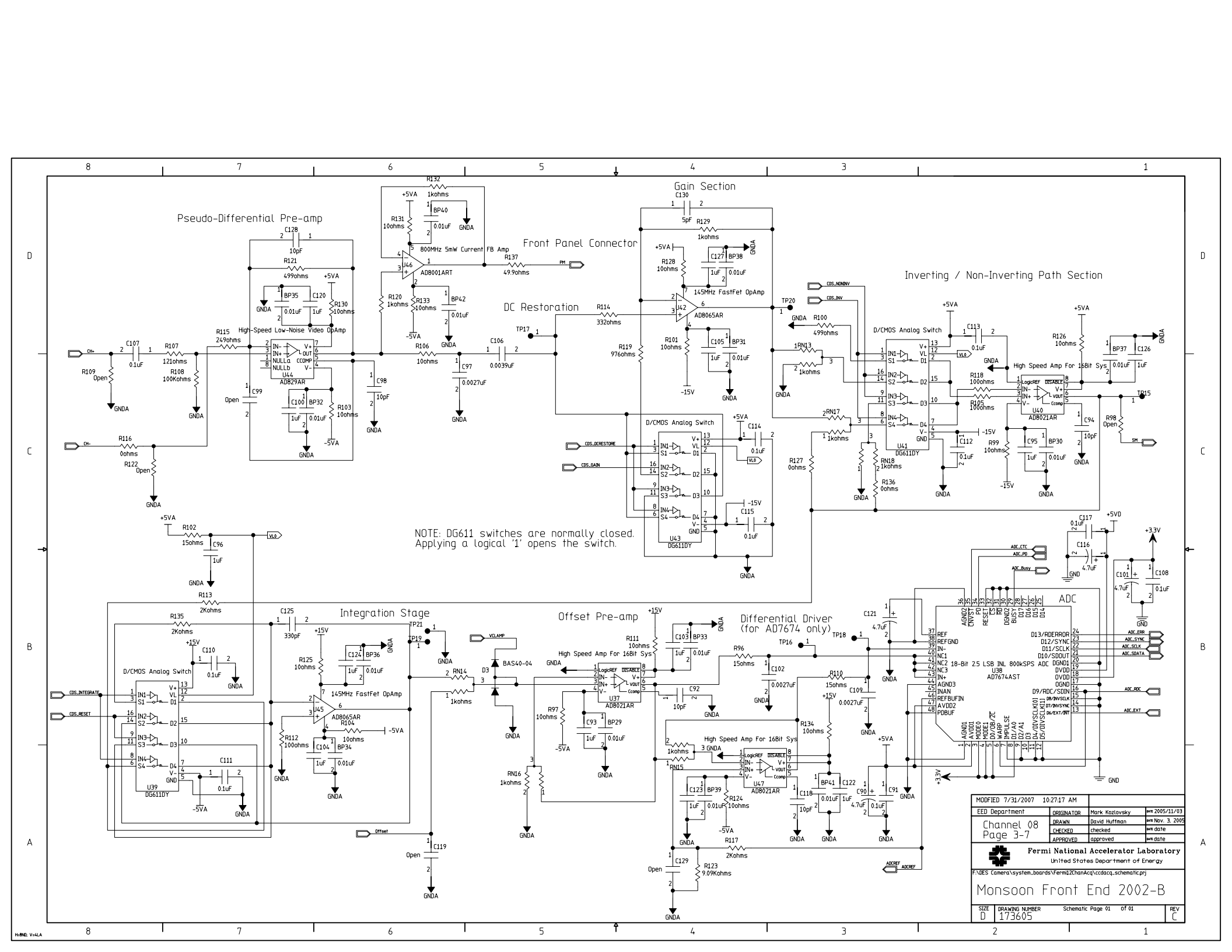
SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		C

H=BND; V=4LA


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
Channel 11
Page 3-10
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
Channel 10
Page 3-9
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
Channel 09
Page 3-8
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Gain Section
Front Panel Connector
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Channel 08
Page 3-7
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
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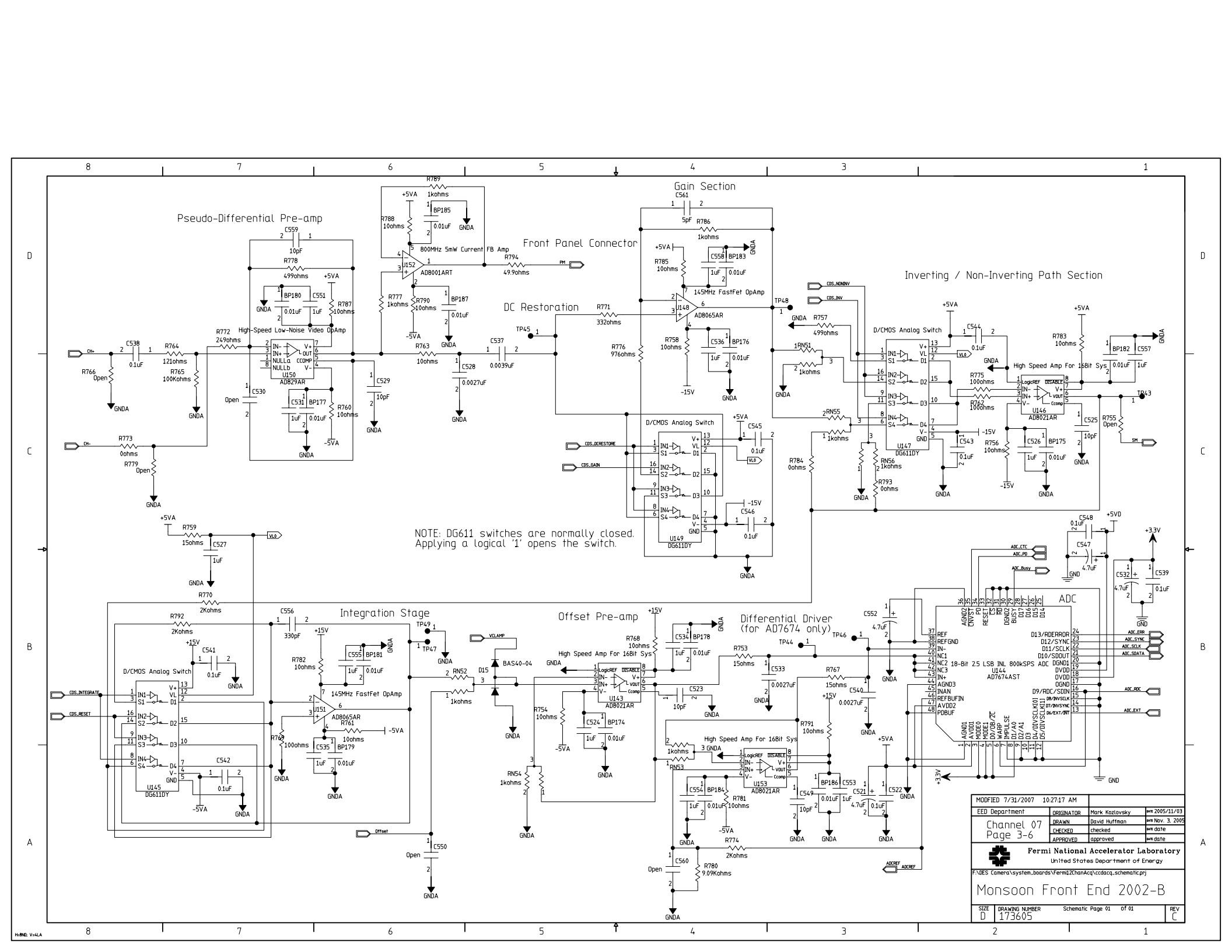
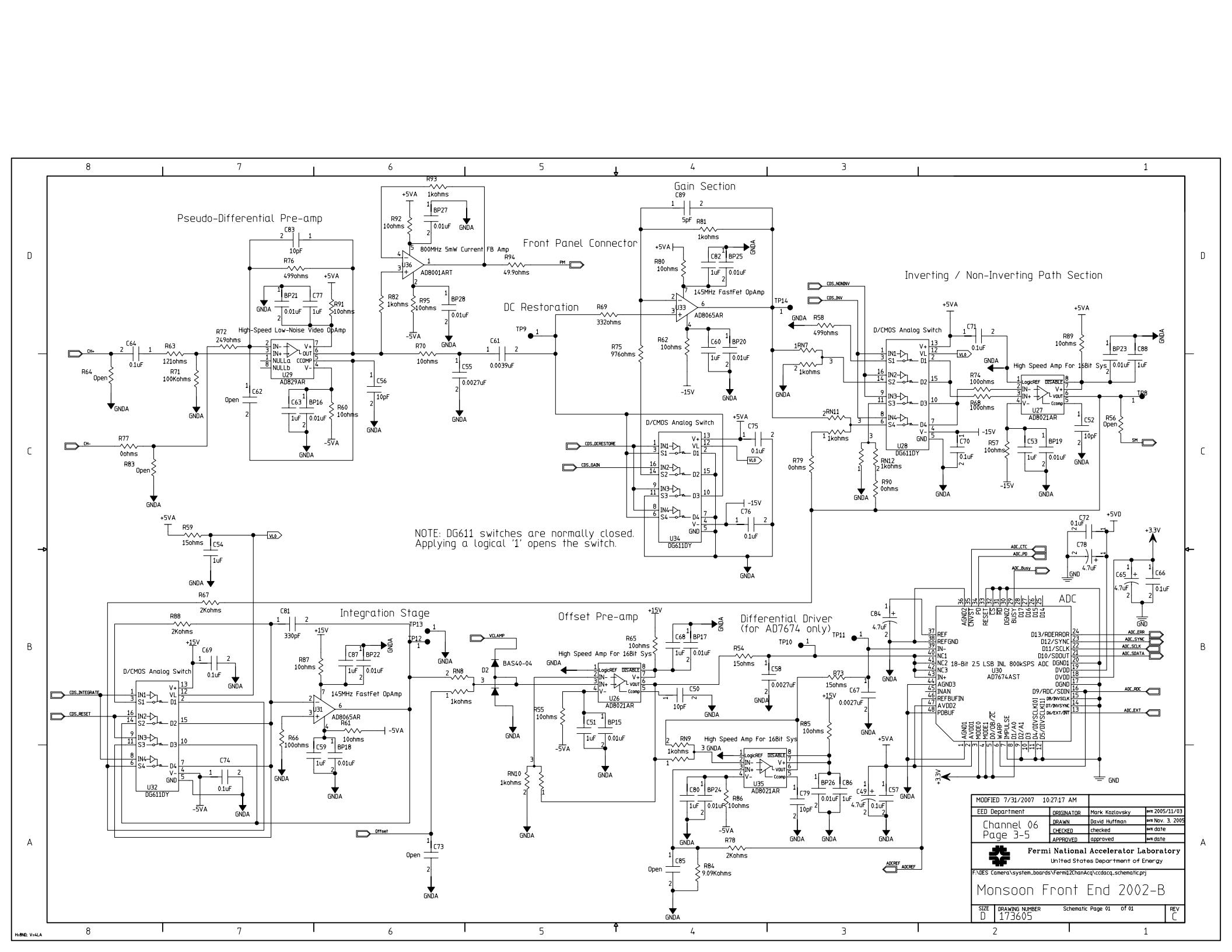
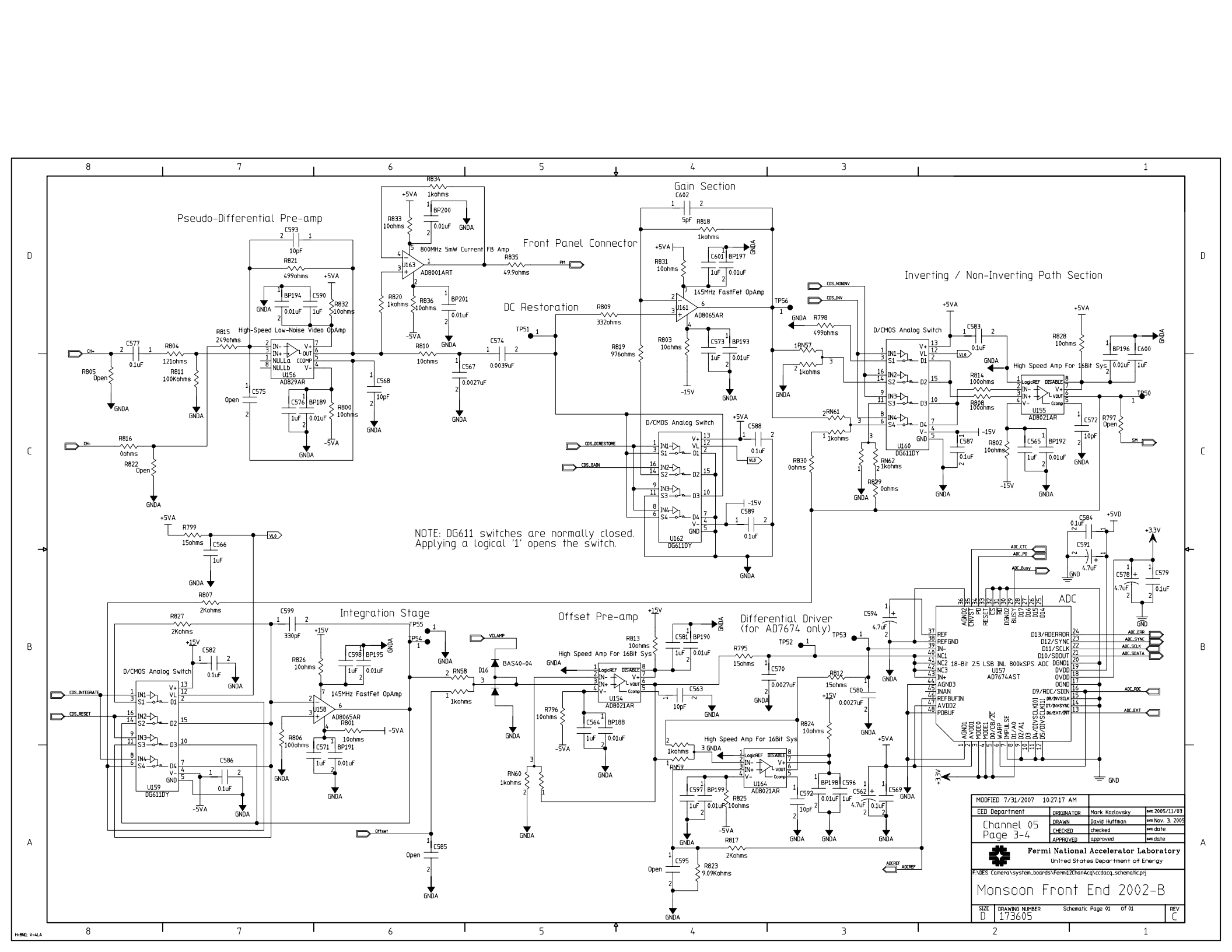
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
High-Speed Low-Noise Video OpAmp
800MHz 5mW Current FB Amp
145MHz FastFet OpAmp
D/CMOS Analog Switch
High Speed Amp For 16Bit Sys
18-Bit 2.5 LSB INL 800kSPS ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
MODIFIED 7/31/2007 10:27:17 AM
EED Department
Channel 07
Page 3-6
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
Channel 06
Page 3-5
Fermi National Accelerator Laboratory
United States Department of Energy
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
BAS40-04
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
MODIFIED 7/31/2007 10:27:17 AM
EED Department
Channel 05
Page 3-4
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Nov. 3, 2005
CHECKED checked date
APPROVED approved date
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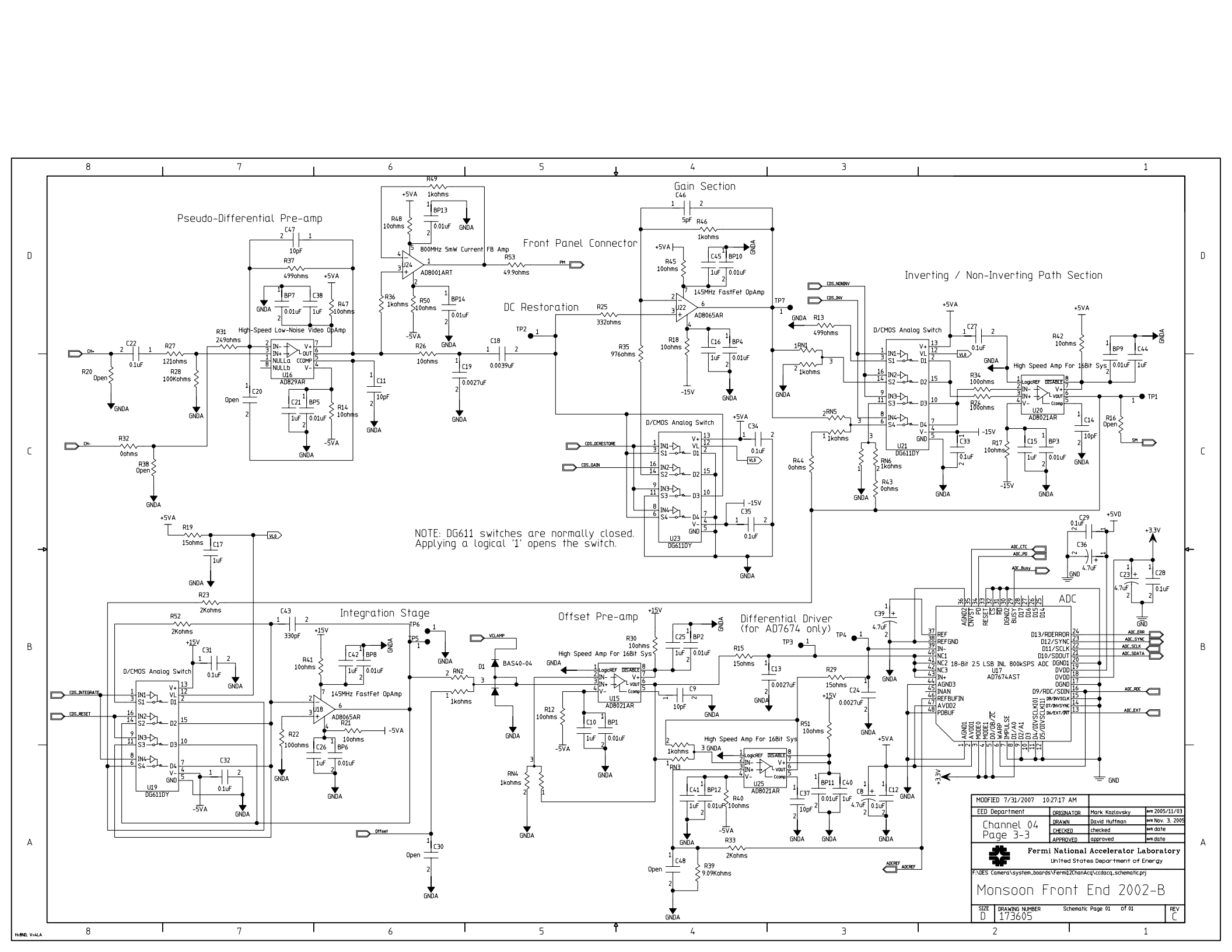
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C


Pseudo-Differential Pre-amp
Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
NOTE: DG611 switches are normally closed.
Applying a logical '1' opens the switch.
800MHz 5mW Current FB Amp
AD8001ART
145MHz FastFet OpAmp
AD8065AR
High-Speed Low-Noise Video OpAmp
AD829AR
High Speed Amp For 16Bit Sys
AD8021AR
D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
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Channel 04
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DRAWN David Huffman date Nov. 3, 2005
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Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER 173605
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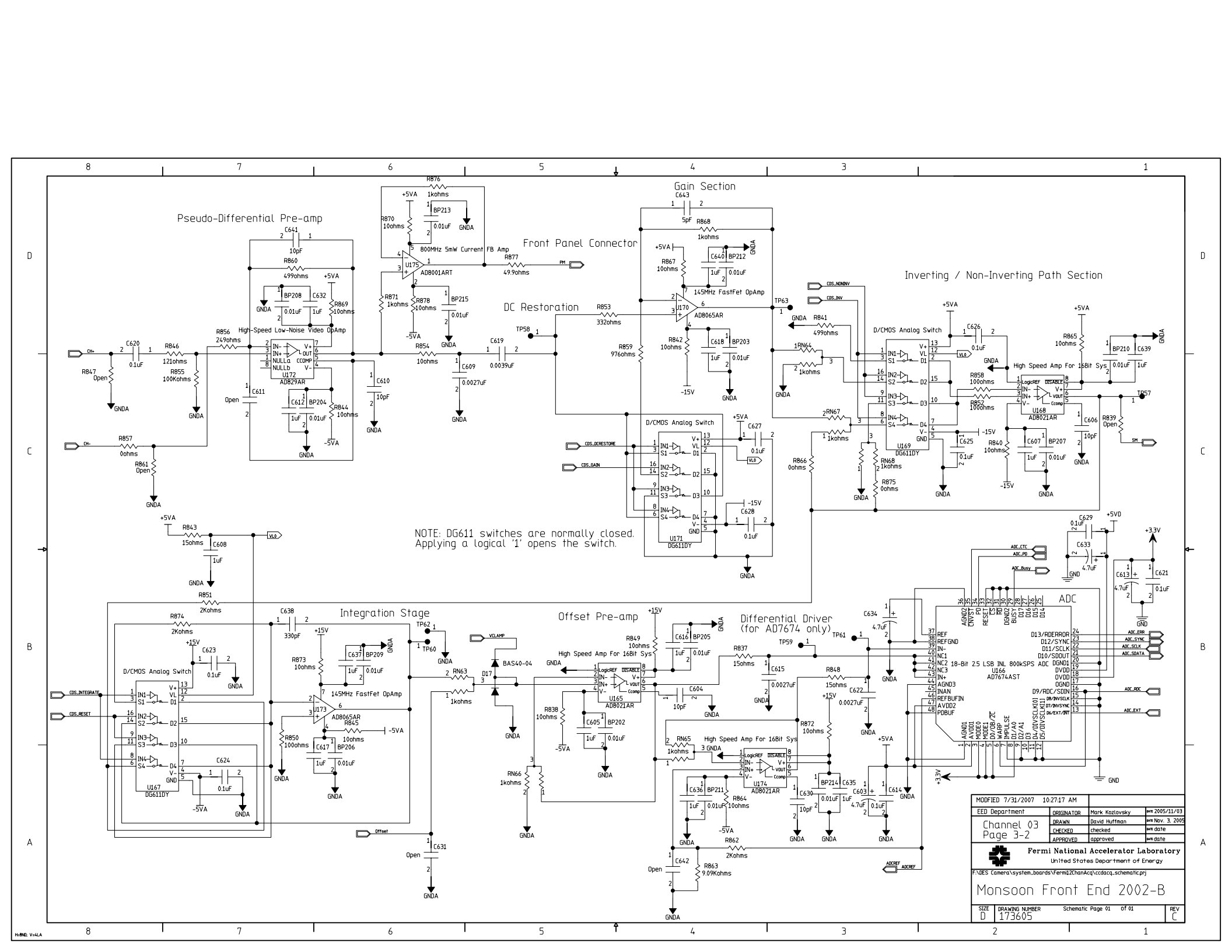
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D/CMOS Analog Switch
DG611DY
18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
BAS40-04
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ORIGINATOR Mark Kozlovsky
Channel 03
Page 3-2
DRAWN David Huffman
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APPROVED approved
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SIZE D
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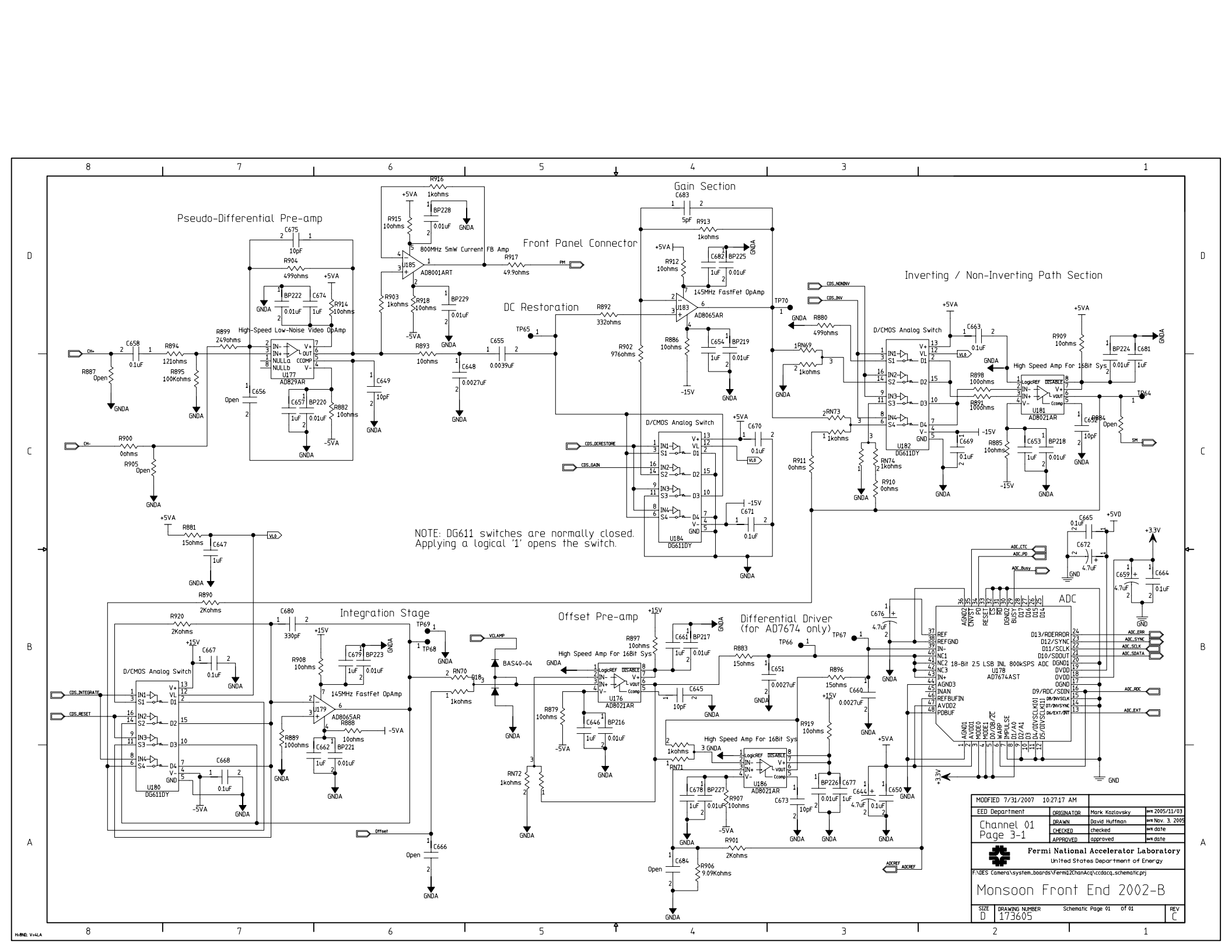
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Front Panel Connector
Gain Section
DC Restoration
Inverting / Non-Inverting Path Section
Integration Stage
Offset Pre-amp
Differential Driver
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DG611DY
High Speed Amp For 16Bit Sys
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18-Bit 2.5 LSB INL 800kSPS ADC
AD7674AST
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Page 3-1
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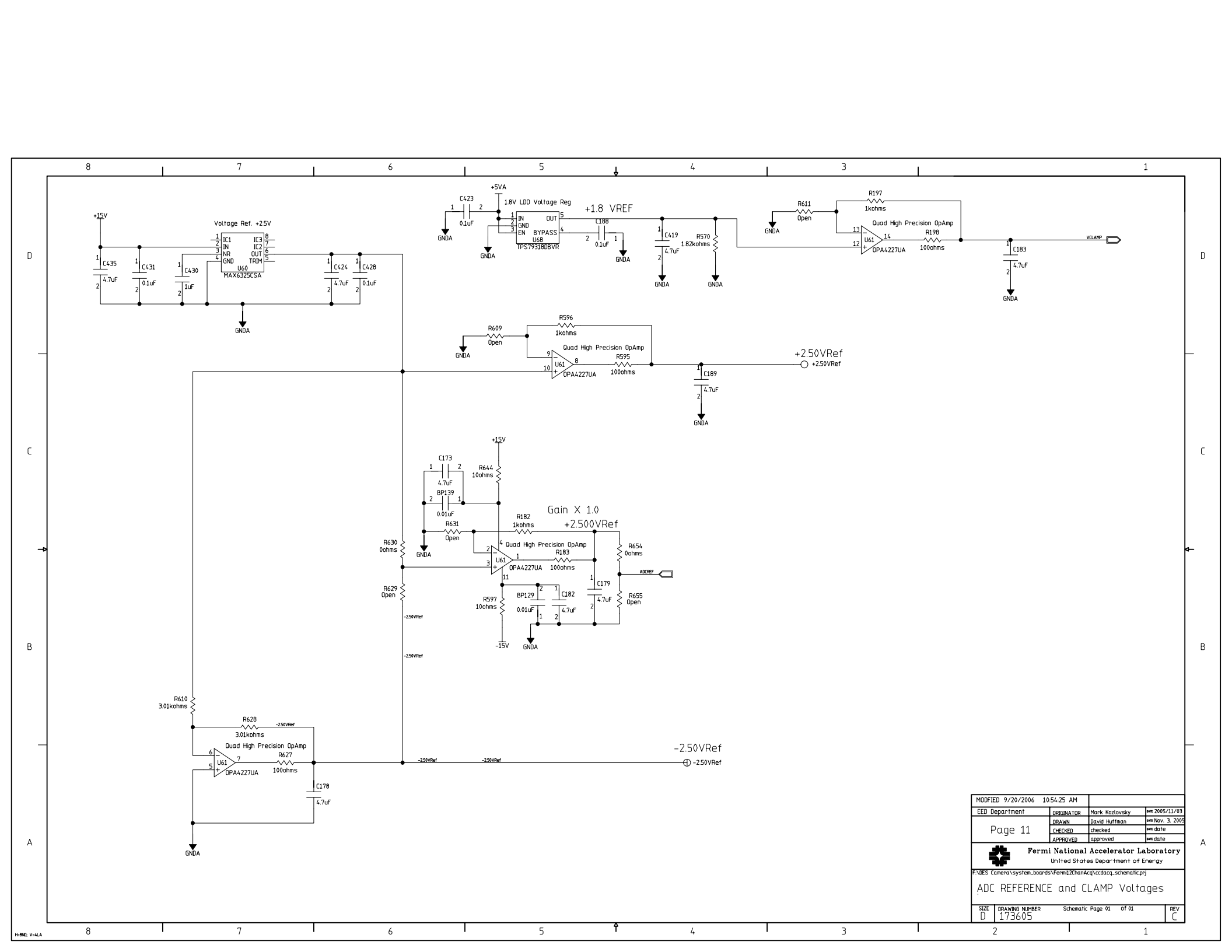

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ADC REFERENCE and CLAMP Voltages

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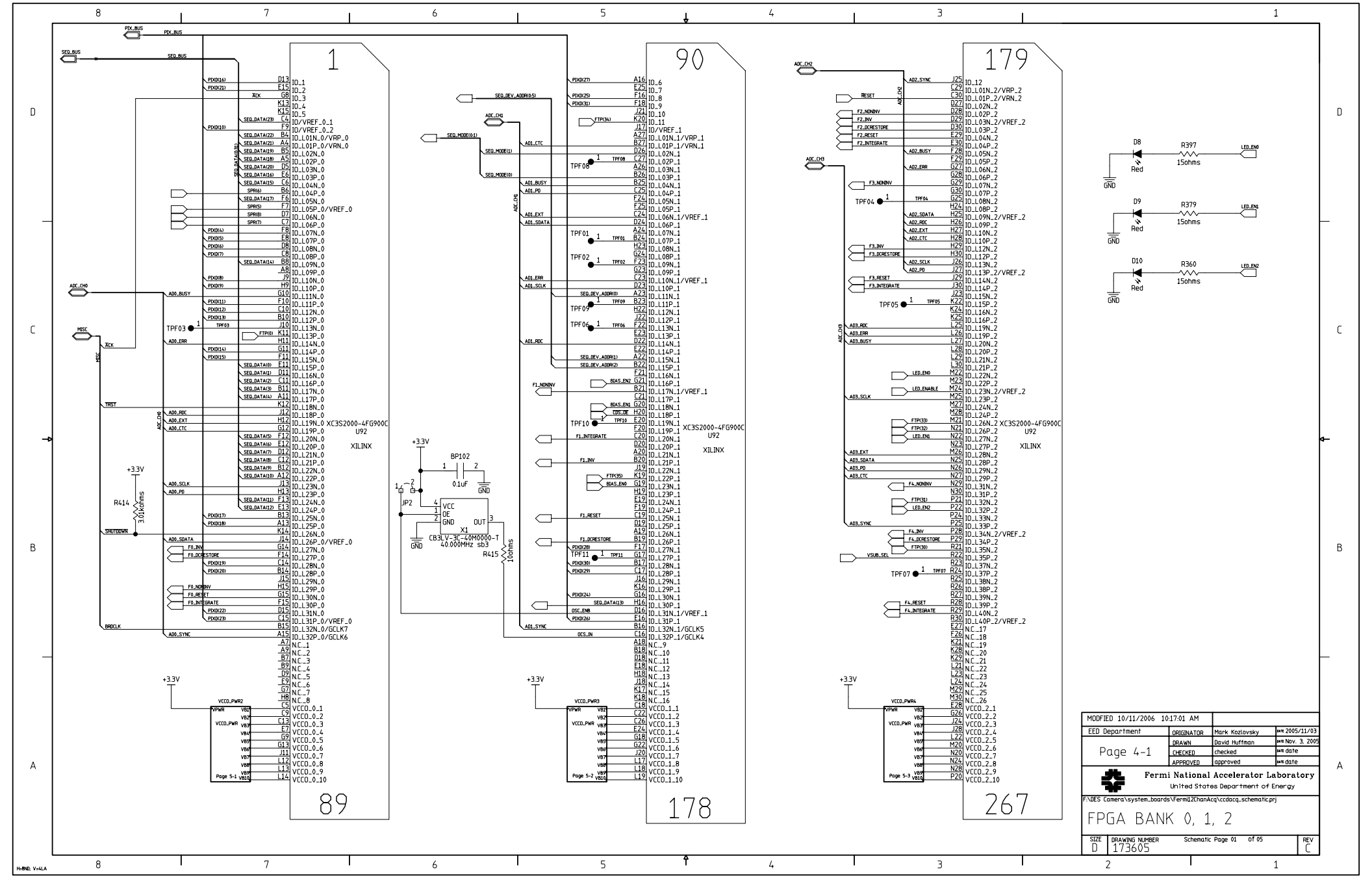
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U92
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Page 4-1
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Nov. 3, 2005
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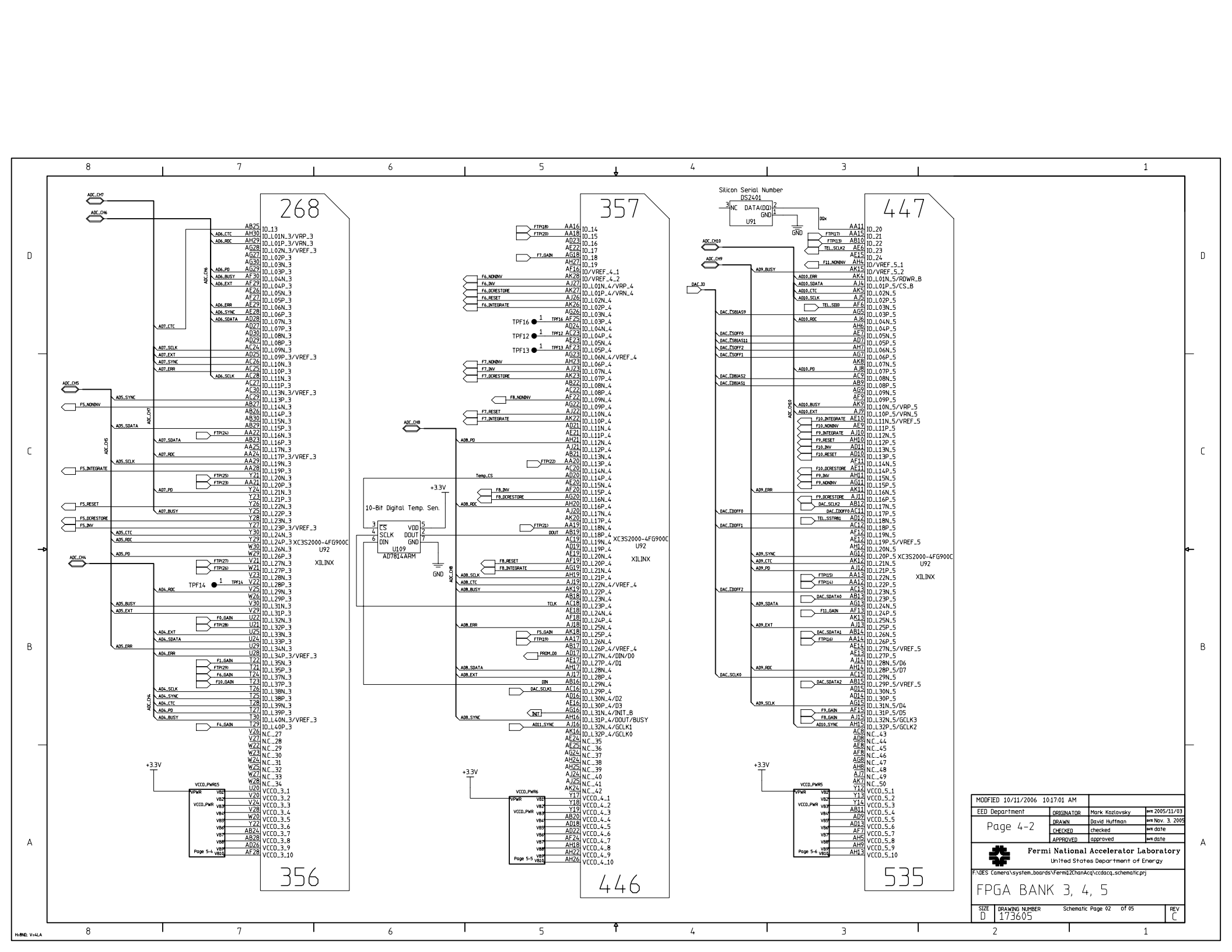
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10-Bit Digital Temp. Sen.
U109
AD7814ARM
Silicon Serial Number
DS2401
U91
+3.3V
GND
FPGA BANK 3, 4, 5
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Page 4-2
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David Huffman
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approved
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Schematic Page 02 of 05
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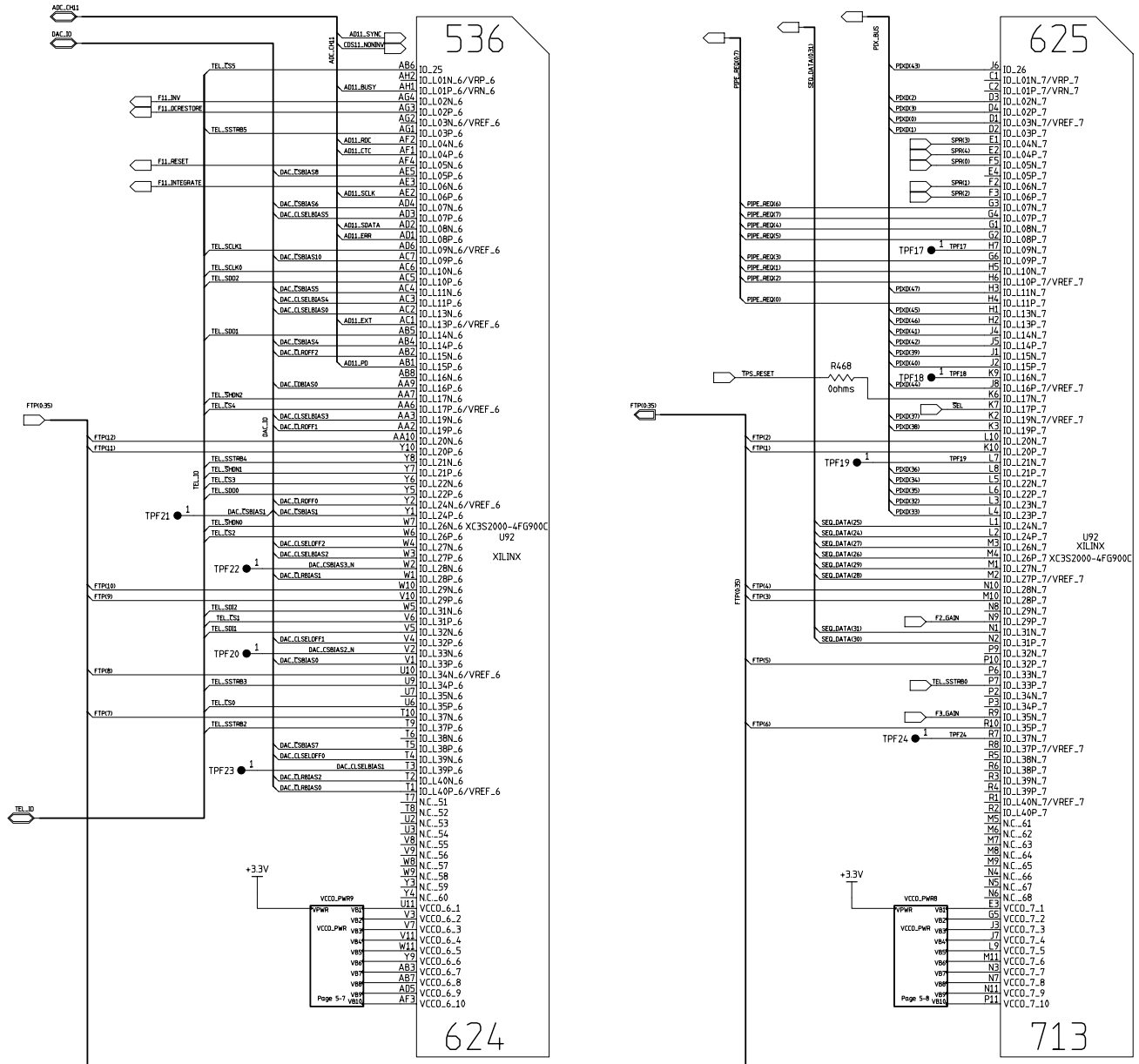

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FPGA BANK 6, 7

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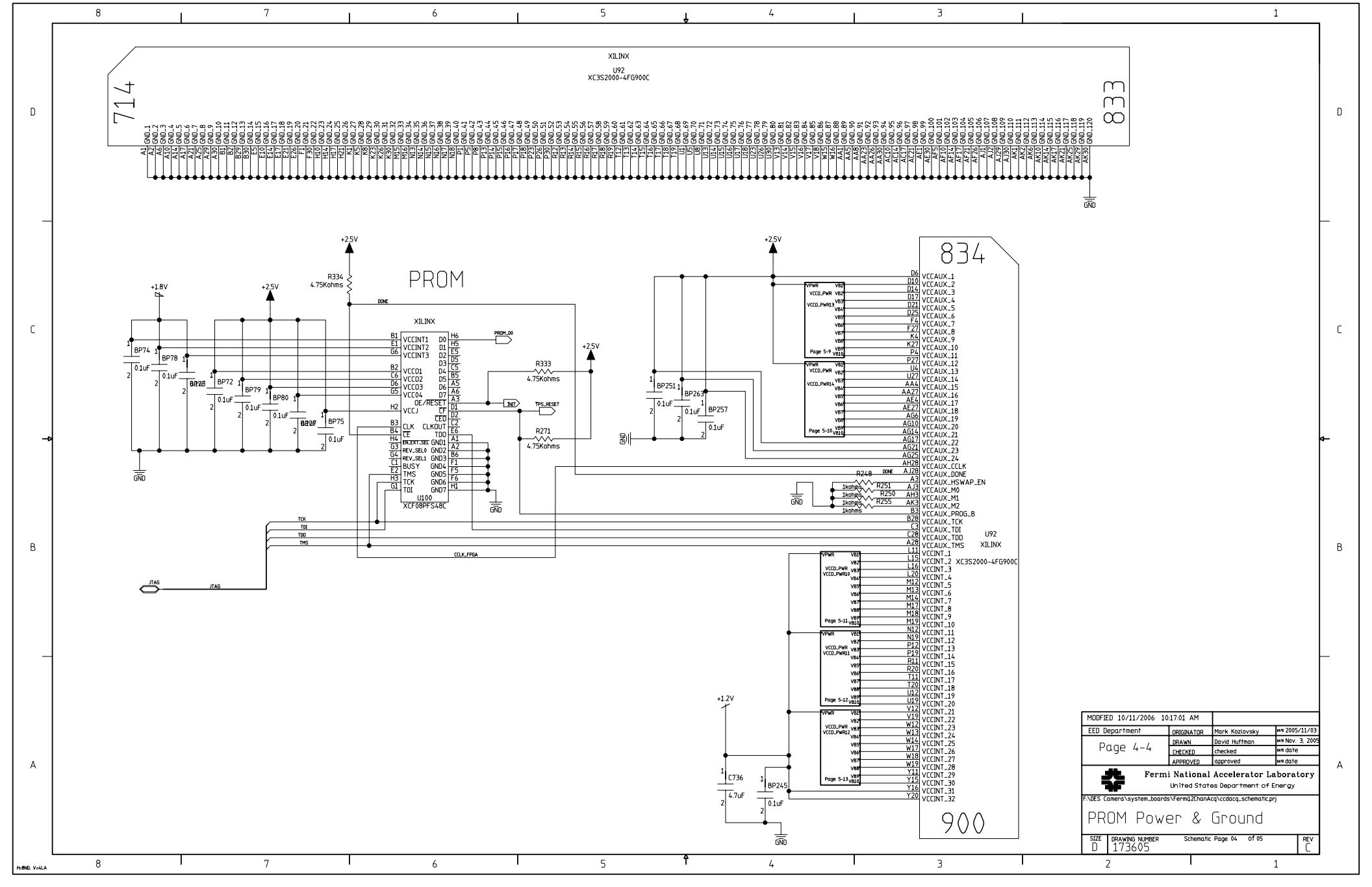

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U92
XC3S2000-4FG900C
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833
834
900
PROM
XILINX
U100
XCF08PFS48C
R334
4.75Kohms
R333
4.75Kohms
R271
4.75Kohms
+2.5V
+1.8V
+1.2V
GND
JTAG
TCK
TDI
TDO
TMS
CCLK_FPGA
PROM_D0
TPS_RESET
INIT
DONE
VCCAUX_1
VCCAUX_2
VCCAUX_3
VCCAUX_4
VCCAUX_5
VCCAUX_6
VCCAUX_7
VCCAUX_8
VCCAUX_9
VCCAUX_10
VCCAUX_11
VCCAUX_12
VCCAUX_13
VCCAUX_14
VCCAUX_15
VCCAUX_16
VCCAUX_17
VCCAUX_18
VCCAUX_19
VCCAUX_20
VCCAUX_21
VCCAUX_22
VCCAUX_23
VCCAUX_24
VCCAUX_CCLK
VCCAUX_DONE
VCCAUX_HSWAP_EN
VCCAUX_M0
VCCAUX_M1
VCCAUX_M2
VCCAUX_PROG_B
VCCAUX_TCK
VCCAUX_TDI
VCCAUX_TDO
VCCAUX_TMS
VCCINT_1
VCCINT_2
VCCINT_3
VCCINT_4
VCCINT_5
VCCINT_6
VCCINT_7
VCCINT_8
VCCINT_9
VCCINT_10
VCCINT_11
VCCINT_12
VCCINT_13
VCCINT_14
VCCINT_15
VCCINT_16
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BP80
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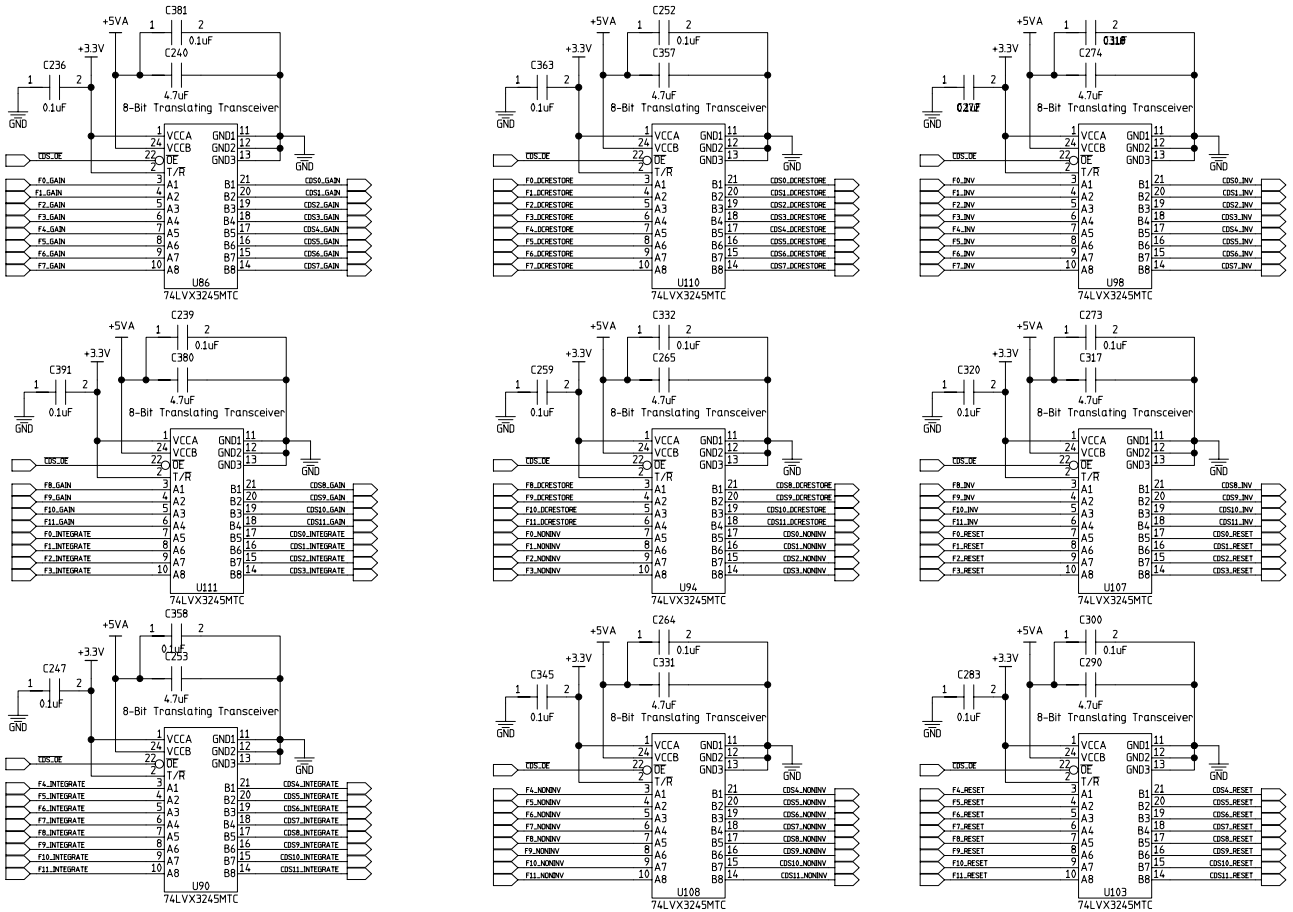
PROM Power & Ground
SIZE D
DRAWING NUMBER 173605
Schematic Page 04 of 05
REV C
H=BND; V=4LA



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Level Translators

SIZE	DRAWING NUMBER	Schematic Page 05 of 05	REV
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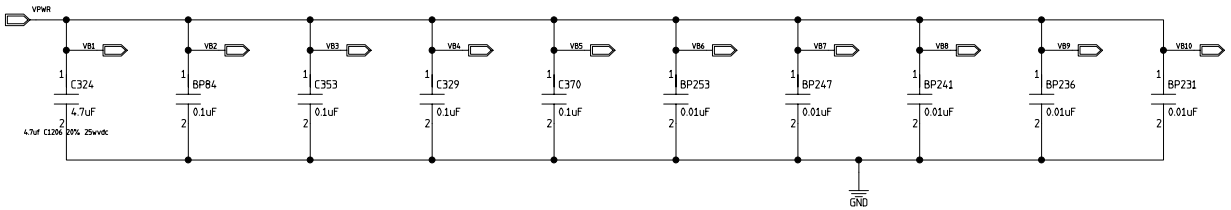

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Power Rail By-Passing

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D	173605	Schematic Page 01 of 01	C

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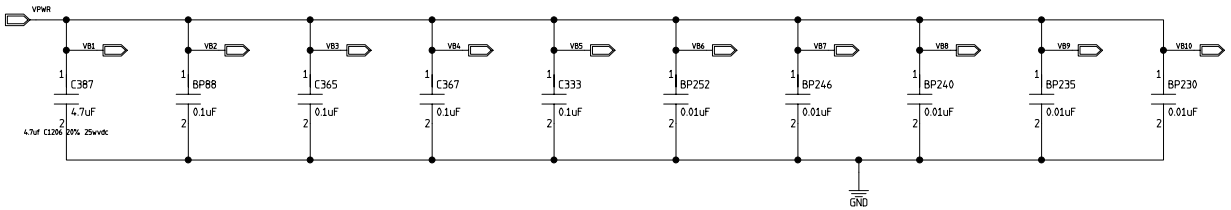

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Power Rail By-Passing

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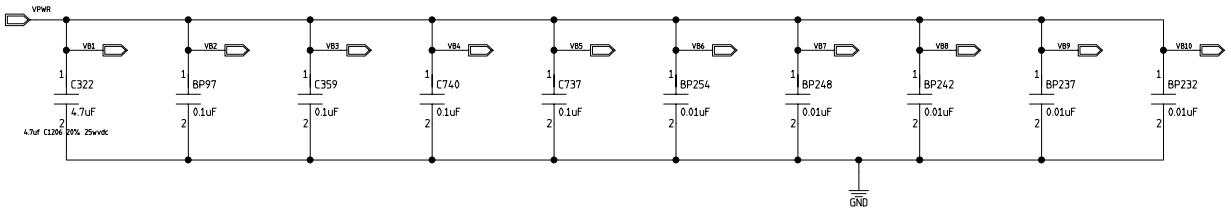

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Power Rail By-Passing

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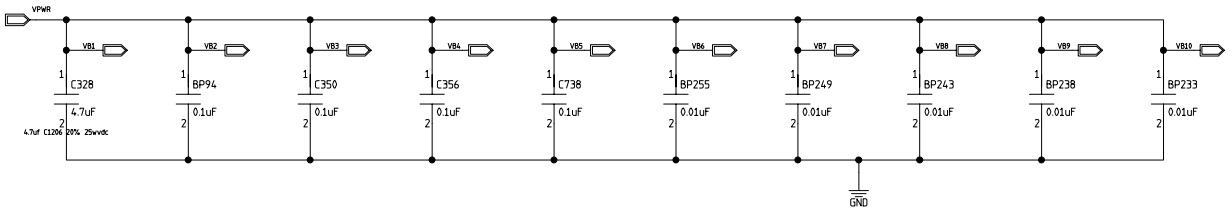

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Power Rail By-Passing

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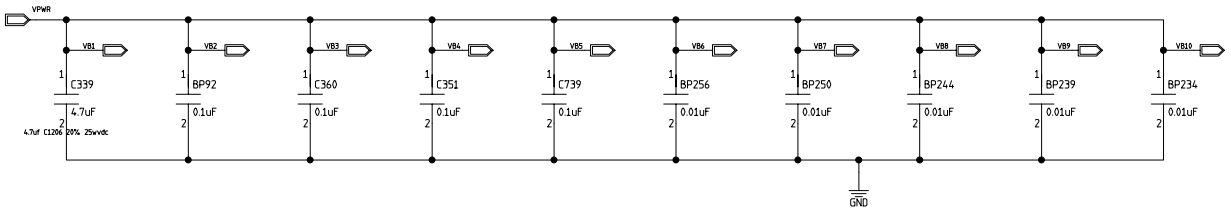

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Power Rail By-Passing

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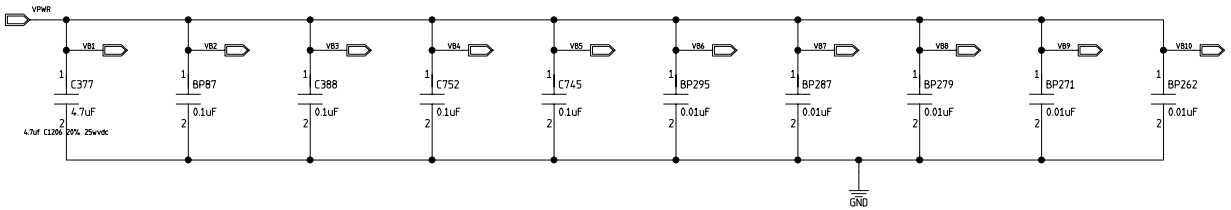

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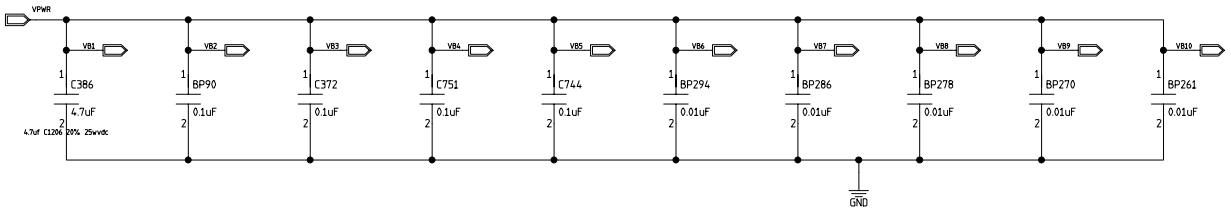

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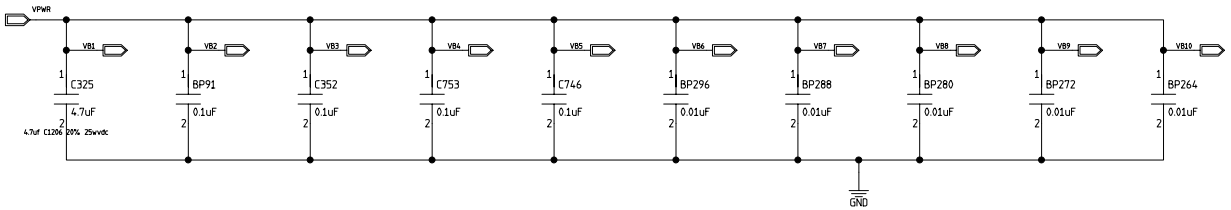

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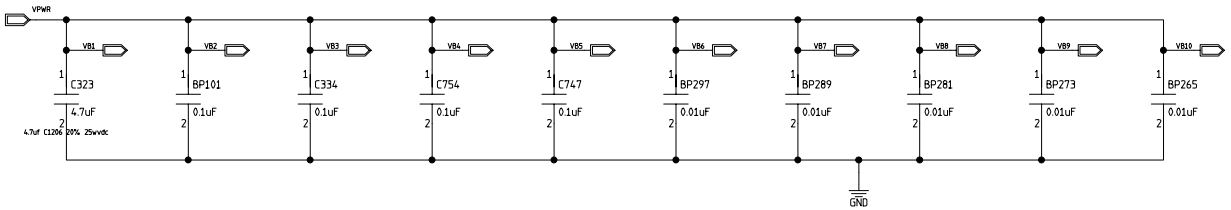

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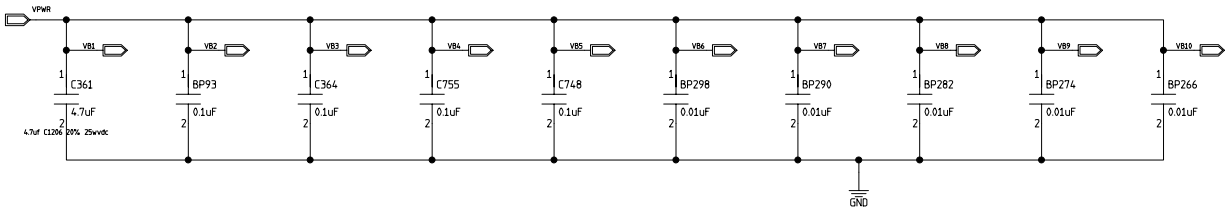

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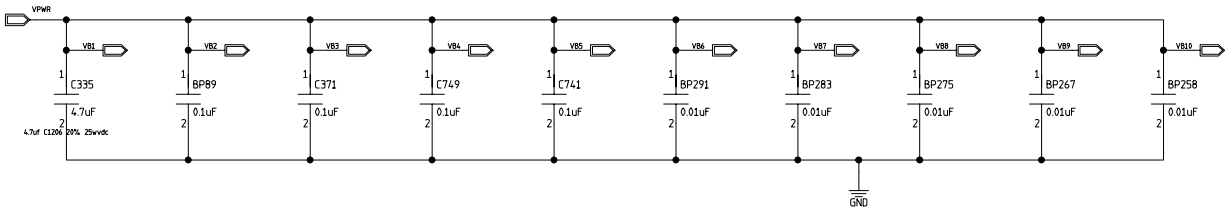

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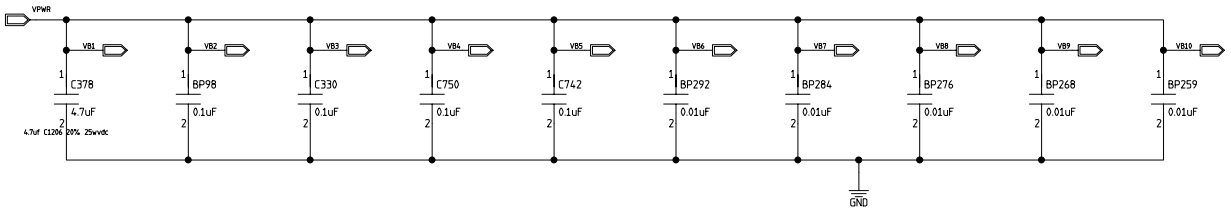

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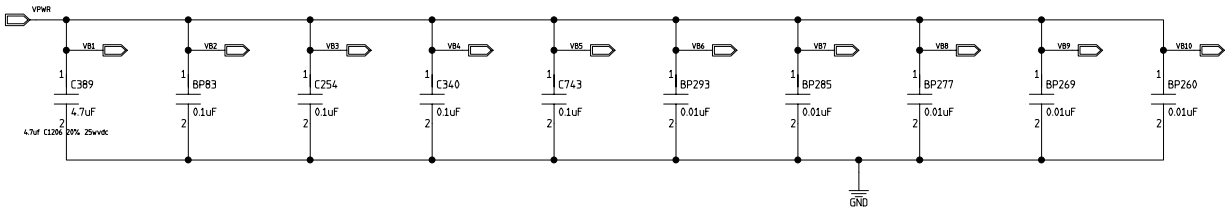

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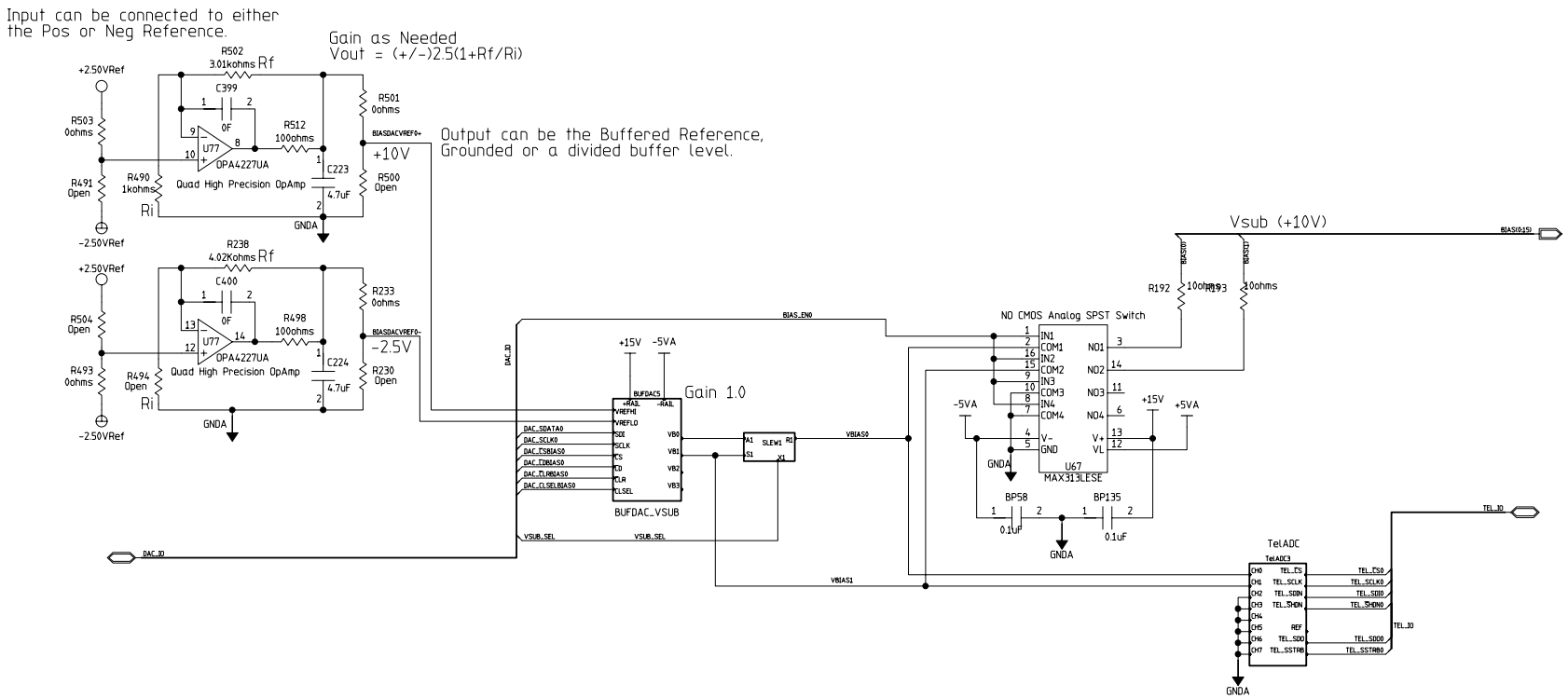
H=BND: V=4LA



MODIFIED 9/20/2006 10:54:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 9	DRAWN	David Huffman	DATE Nov. 3, 2005
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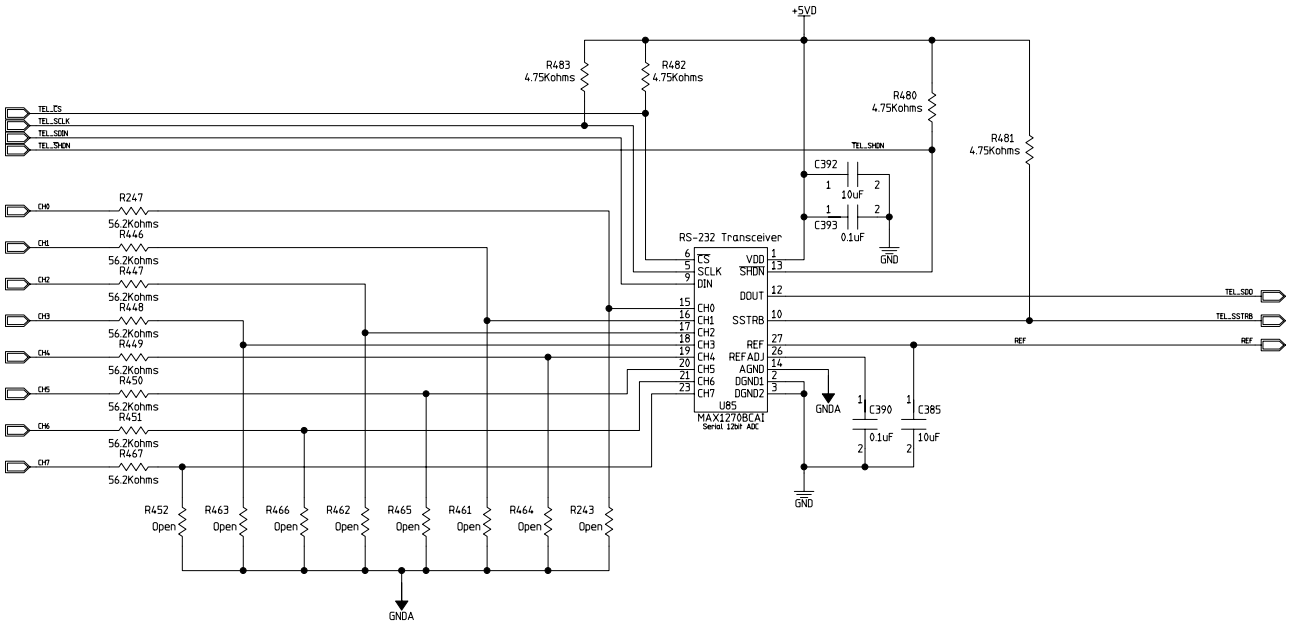
Bias Output w/Enable 1-16

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 0-7

MODFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7-2	DRAWN	David Huffman	DATE Nov. 3, 2005
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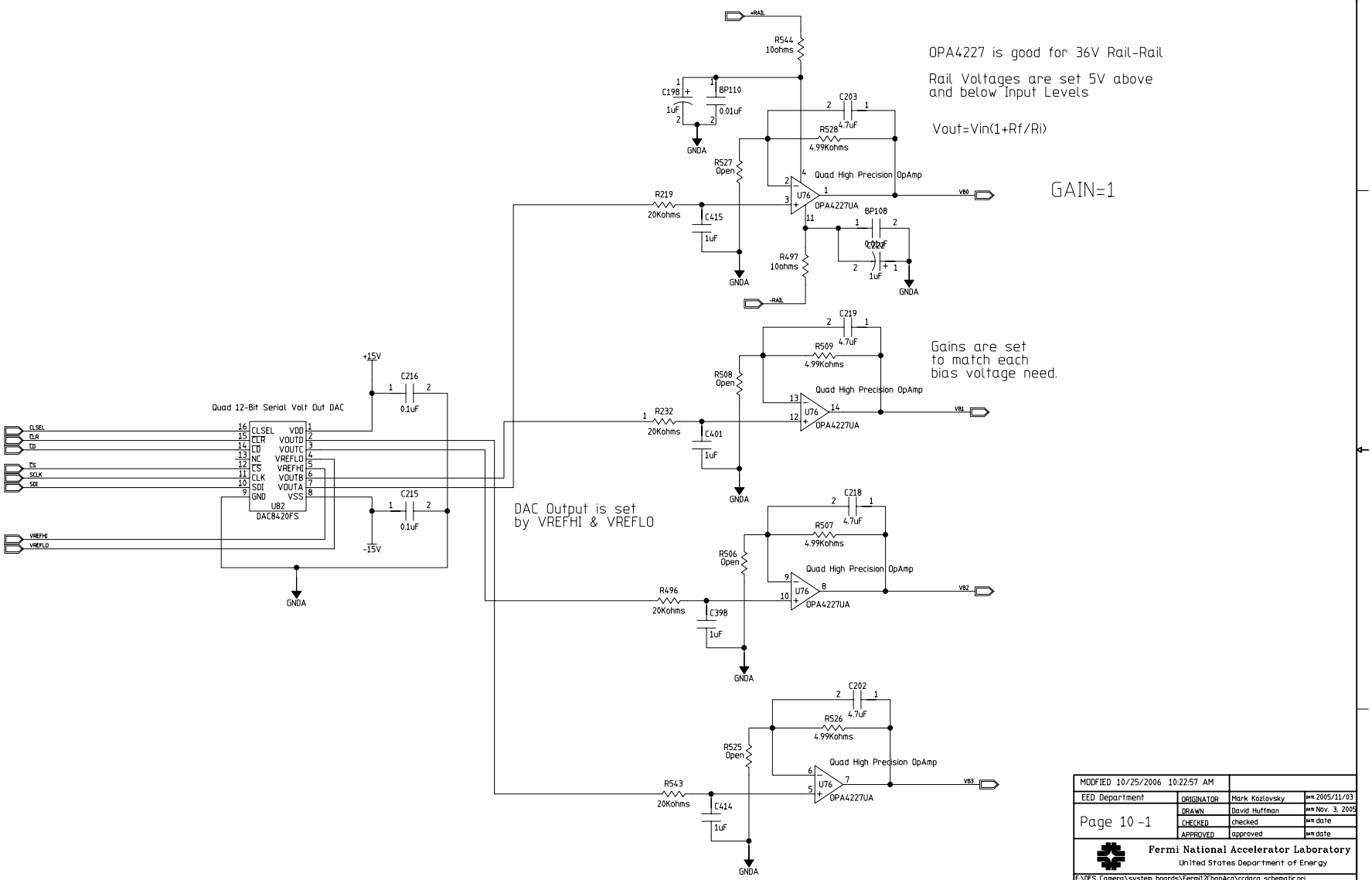
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 Of 01	C

H=BND: V=4LA


OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1
Gains are set to match each bias voltage need.
DAC Output is set by VREFHI & VREFLO
Quad 12-Bit Serial Volt Out DAC
DAC8420FS
Quad High Precision OpAmp
OPA4227UA
+RAIL
-RAIL
+15V
-15V
GNDA
R544 10ohms
R528 4.99Kohms
R527 Open
R219 20Kohms
R497 10ohms
R509 4.99Kohms
R508 Open
R232 20Kohms
R507 4.99Kohms
R506 Open
R496 20Kohms
R526 4.99Kohms
R525 Open
R543 20Kohms
C198 1uF
BP110 0.01uF
C203 4.7uF
C415 1uF
BP108 0.01uF
C219 4.7uF
C216 0.1uF
C401 1uF
C218 4.7uF
C215 0.1uF
C398 1uF
C202 4.7uF
C414 1uF
U76
U82
VB0
VB1
VB2
VB3
CLSEL
CLR
CD
TS
SCLK
SDI
VREFHI
VREFLO
MODIFIED 10/25/2006 10:22:57 AM
EED Department
Page 10 -1
ORIGINATOR Mark Kozlovsky 2005/11/03
DRAWN David Huffman Nov. 3, 2005
CHECKED checked date
APPROVED approved date
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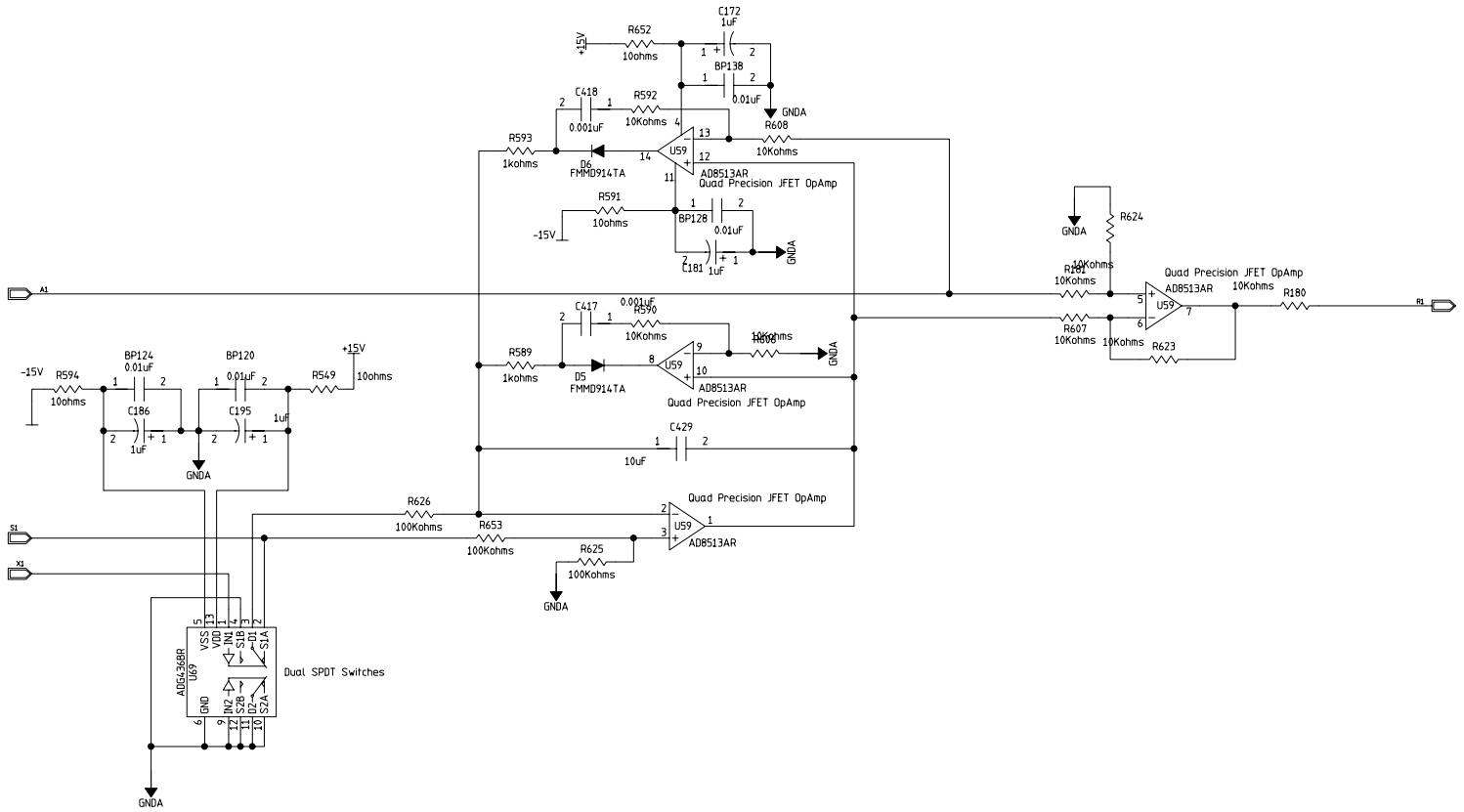
F:\DES Camera\system_boards\Fermi12ChanAcq\ccdacq_schematic.prj
4 Channel Buffered DAC - VSUB Ramp Control
BIAS 0,1
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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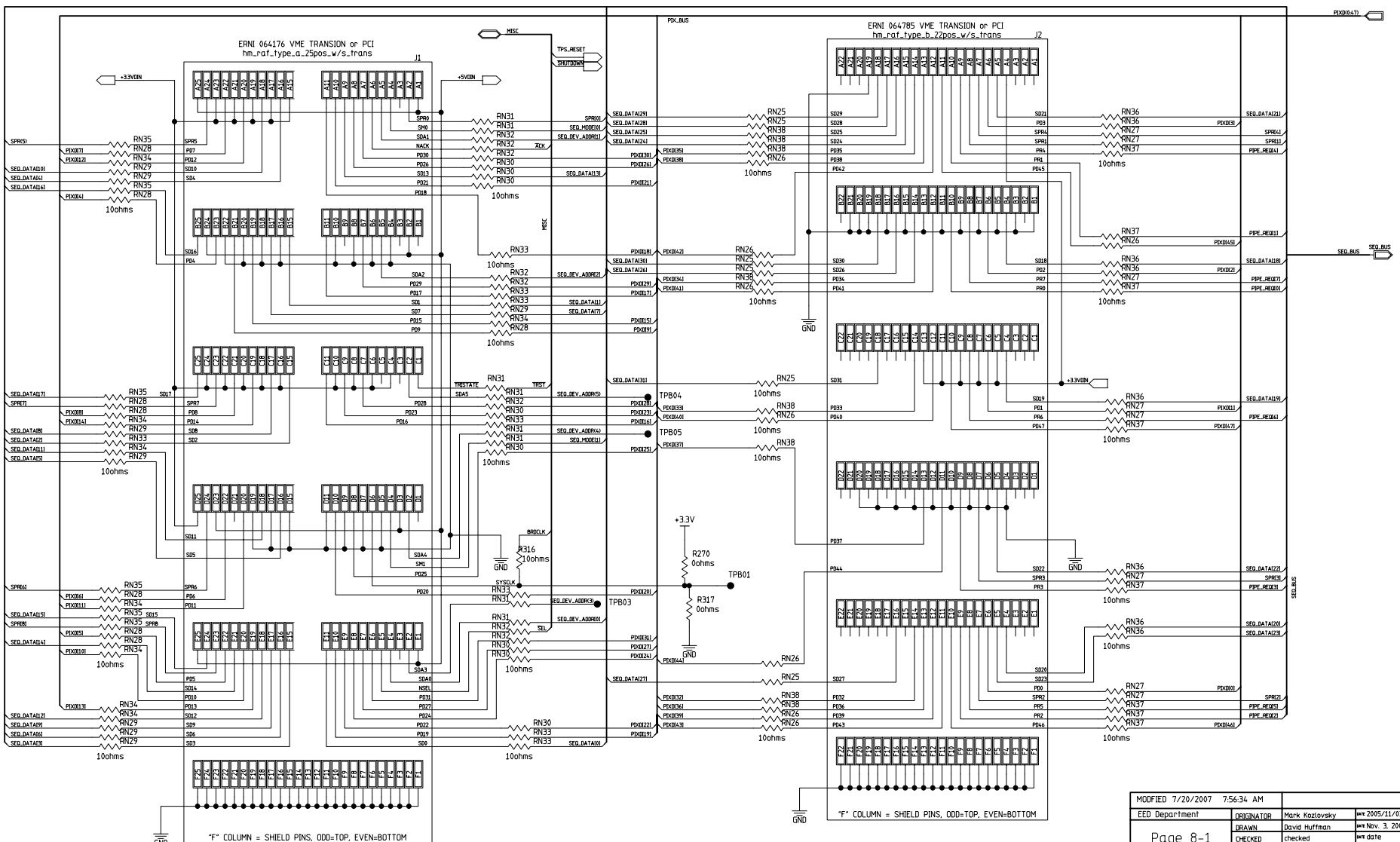
SLEW CONTROL

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C

H=BND: V=4LA



MODFIED 7/20/2007 7:56:34 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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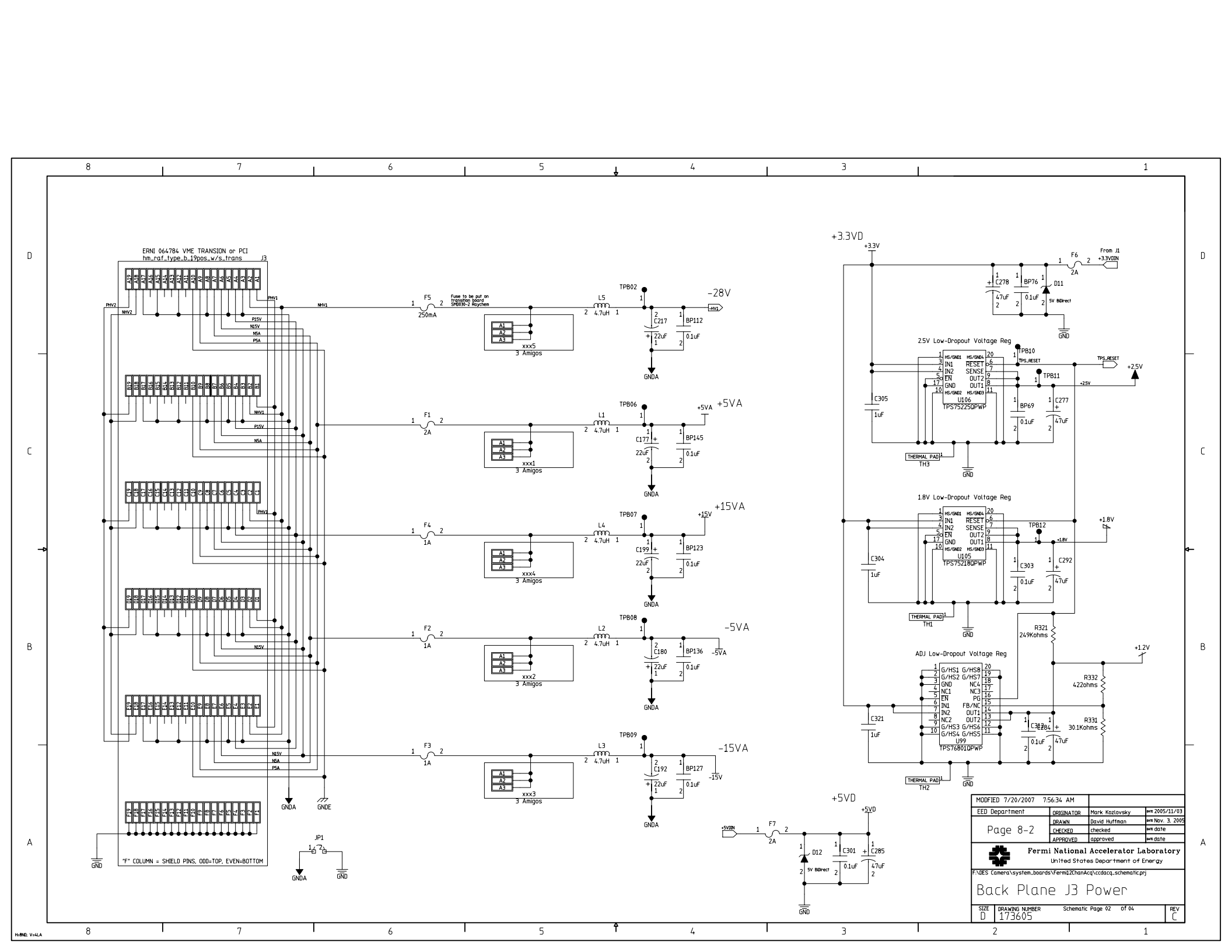
Back Plane J1 J2

SIZE	DRAWING NUMBER	Schematic Page 01 of 04	REV
D	173605		C

H=BND; V=4LA


ERNI 064784 VME TRANSION or PCI
hm_raf_type_b_19pos_w/s_trans
J3
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
PHV1
PHV2
NHV1
NHV2
P15V
N15V
N5A
P5A
GNDA
GNDE
GND
JP1
F5
250mA
Fuse to be put on transition board SMD030-2 Raychem
TPB02
-28V
-HV1
L5
4.7uH
C217
22uF
BP112
0.1uF
xxx5
3 Amigos
F1
2A
TPB06
+5VA
L1
C177
BP145
xxx1
F4
1A
TPB07
+15VA
+15V
L4
C199
BP123
xxx4
F2
TPB08
-5VA
L2
C180
BP136
xxx2
F3
TPB09
-15VA
-15V
L3
C192
BP127
xxx3
+3.3VD
+3.3V
From J1
+3.3VDIN
F6
2A
C278
47uF
BP76
0.1uF
D11
5V BiDirect
2.5V Low-Dropout Voltage Reg
U106
TPS75225QPWP
TPB10
TPS_RESET
TPB11
+2.5V
C305
1uF
BP69
C277
1.8V Low-Dropout Voltage Reg
U105
TPS75218QPWP
TPB12
+1.8V
C304
C303
C292
R321
249Kohms
+1.2V
ADJ Low-Dropout Voltage Reg
U99
TPS76801QPWP
R332
422ohms
R331
30.1Kohms
C321
C284
THERMAL PAD
TH1
TH2
TH3
+5VD
+5VDIN
F7
2A
D12
C301
C285
MODIFIED 7/20/2007 7:56:34 AM
EED Department
Page 8-2
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Nov. 3, 2005
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APPROVED approved date
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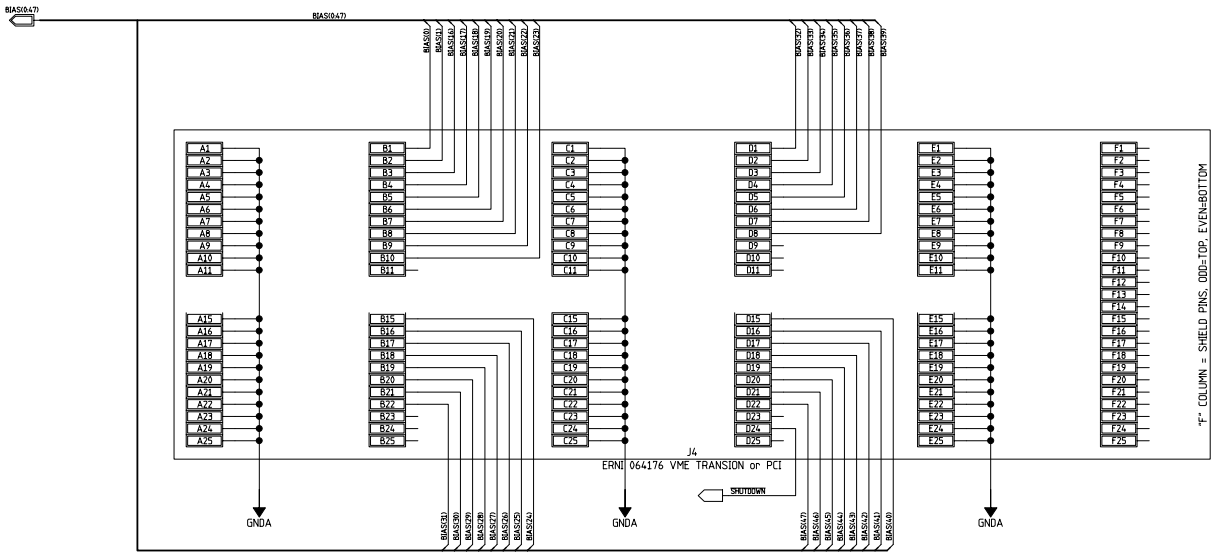
Back Plane J3 Power
SIZE D
DRAWING NUMBER 173605
Schematic Page 02 of 04
REV C



MODIFIED 7/20/2007 7:56:34 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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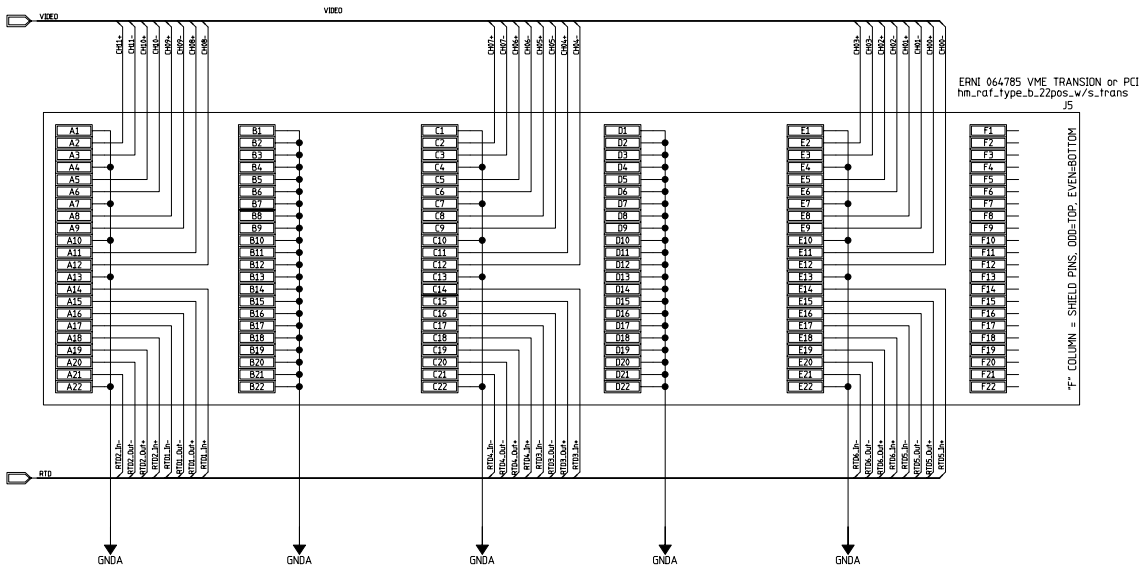
DIGITAL OUTPUTS & BIAS J4

SIZE	DRAWING NUMBER	Schematic Page 03 of 04	REV
D	173605		C

H=BND, V=4LA



MODIFIED 7/20/2007 7:56:34 AM			
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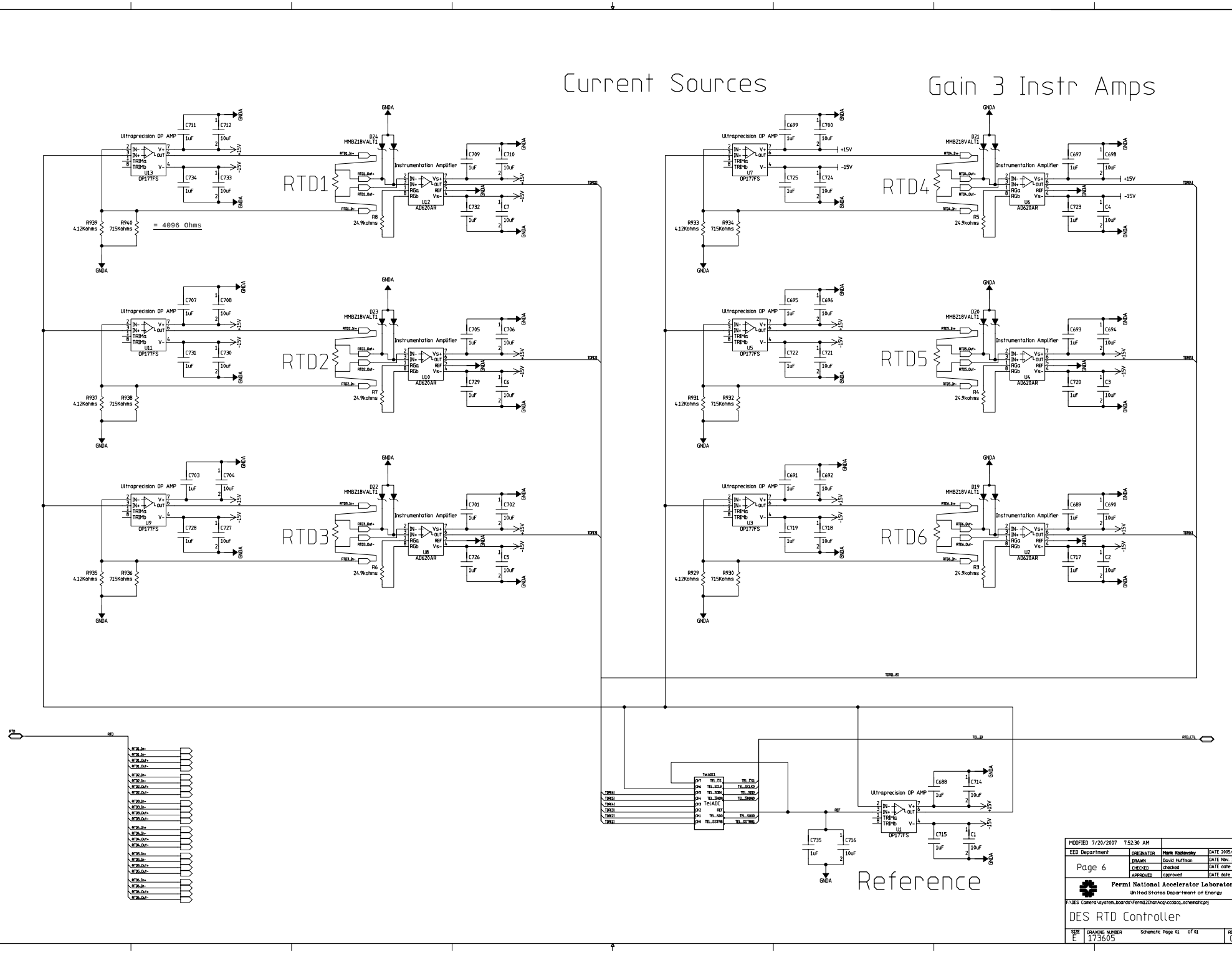
VIDEO INPUTS & RTD INPUTS J5

SIZE	DRAWING NUMBER	Schematic Page 04 of 04	REV
D	173605		C



MODIFIED 7/20/2007 7:52:30 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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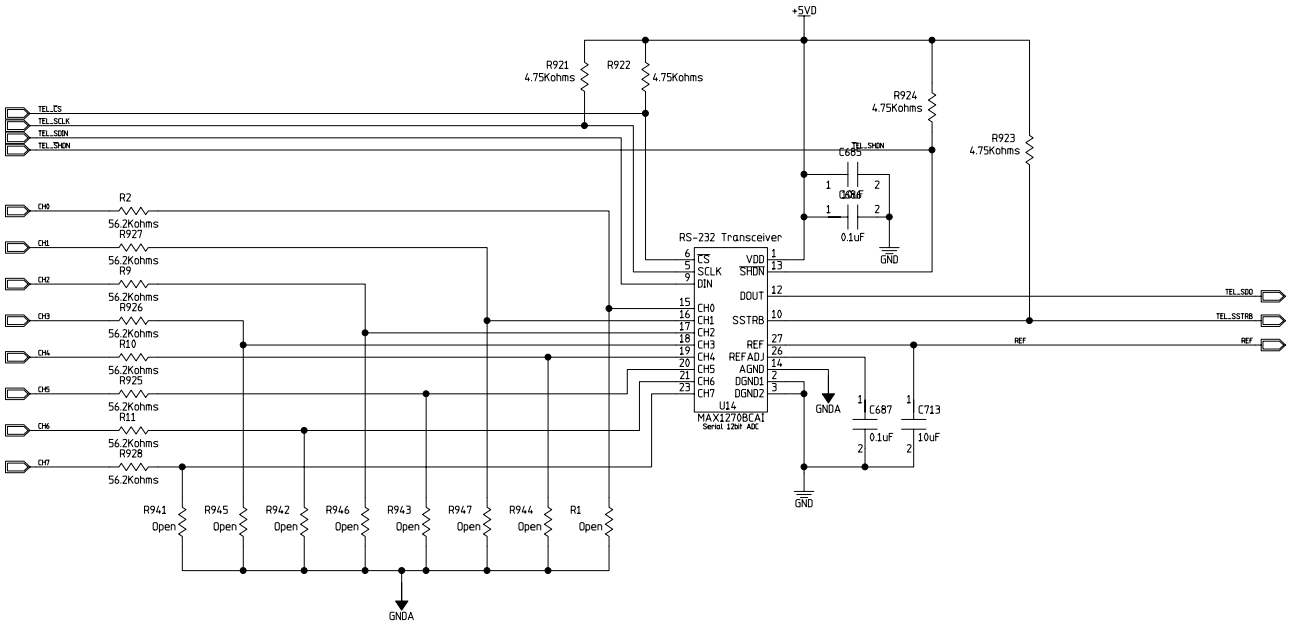
DES RTD Controller

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
E	173605		C



RTD ADCs

MODFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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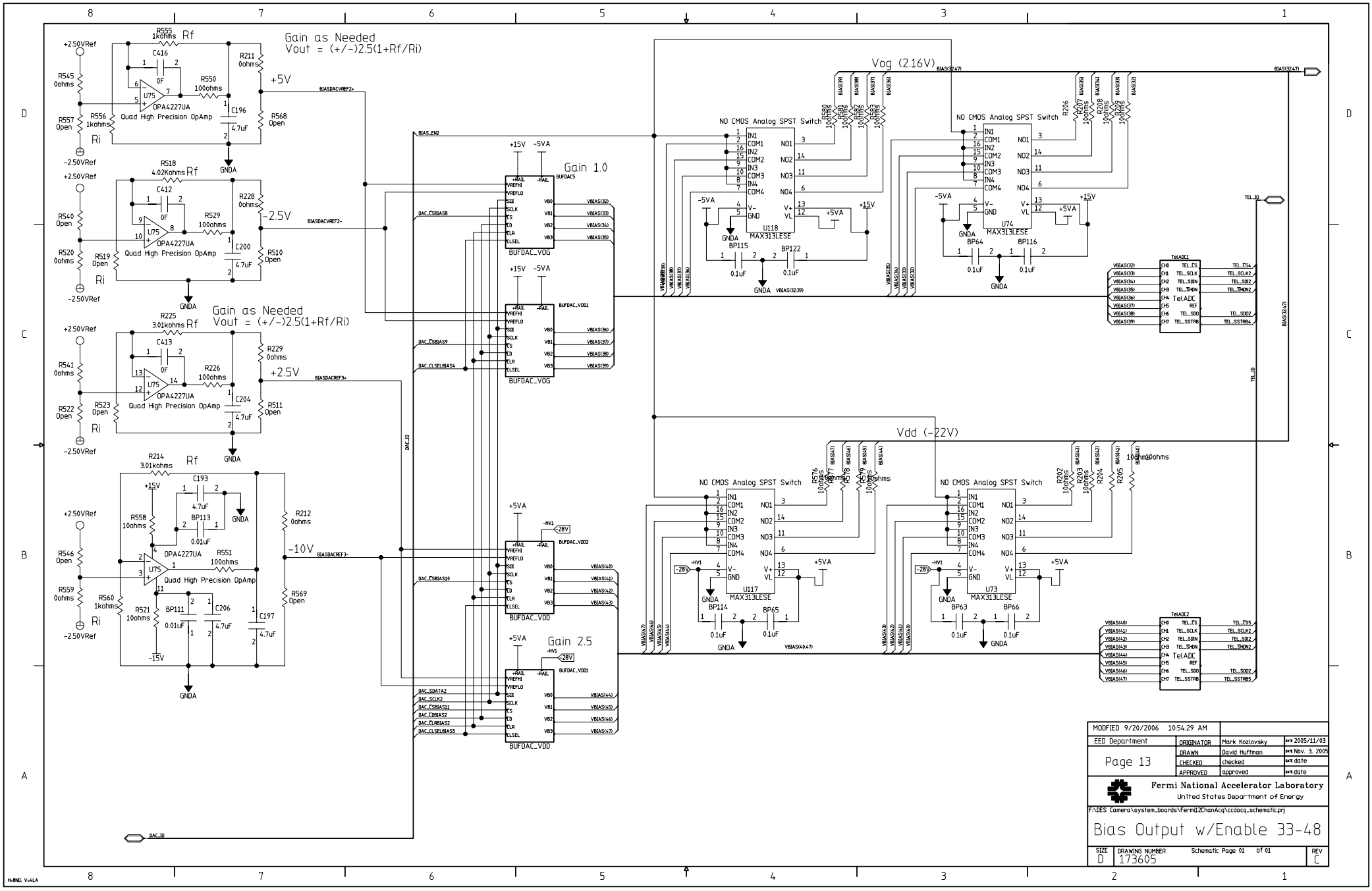
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	Schematic Page 01 Of 01	REV
D	173605		C

H:BND: V:4LA


Gain as Needed
Vout = (+/-)2.5(1+Rf/Ri)
Gain 1.0
Gain as Needed
Vout = (+/-)2.5(1+Rf/Ri)
Vog (2.16V)
Vdd (-22V)
Gain 2.5
Quad High Precision OpAmp
OPA4227UA
NO CMOS Analog SPST Switch
MAX313LESE
BUFDAC5
BUFDAC_VOG
BUFDAC_VOG1
BUFDAC_VDD2
BUFDAC_VDD1
BUFDAC_VDD
TelADC1
TelADC2
TelADC
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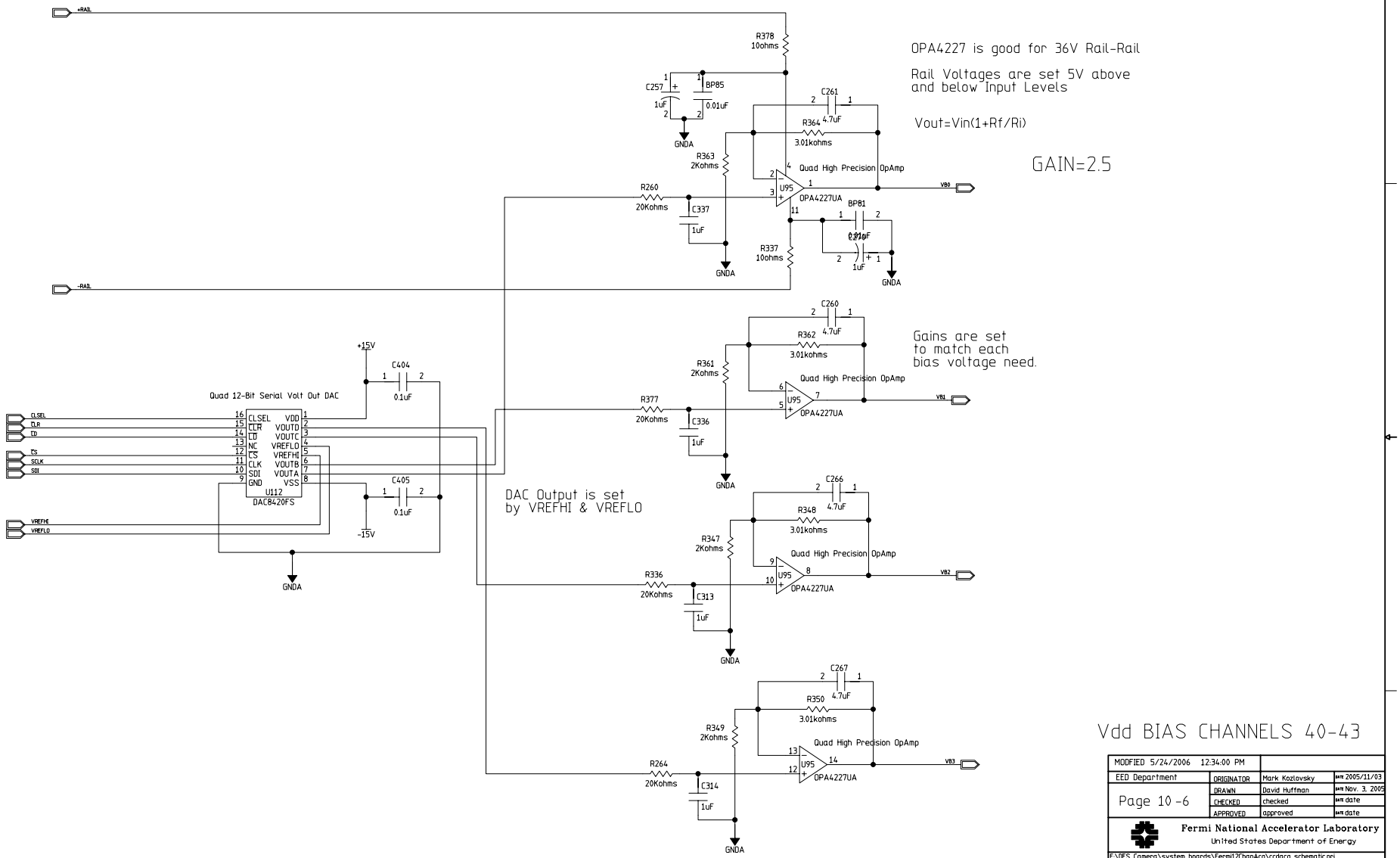
Bias Output w/Enable 33-48
MODIFIED 9/20/2006 10:54:29 AM
EED Department
Page 13
ORIGINATOR Mark Kozlovsky
DRAWN David Huffman
CHECKED checked
APPROVED approved
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



Vdd BIAS CHANNELS 40-43

MODIFIED 5/24/2006 12:34:00 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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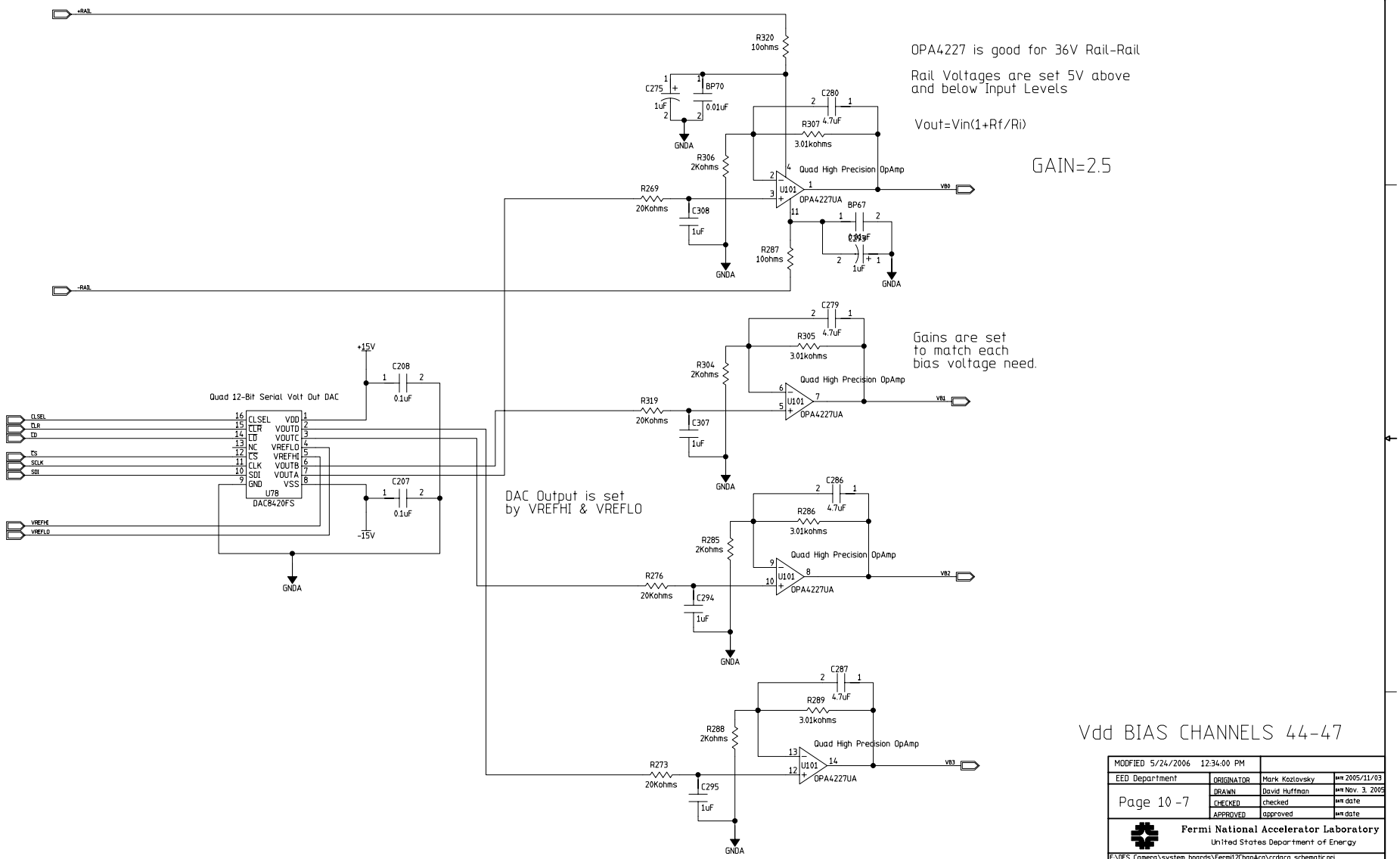
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C



MODIFIED 5/24/2006 12:34:00 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 10 -7	DRAWN	David Huffman	DATE Nov. 3, 2005
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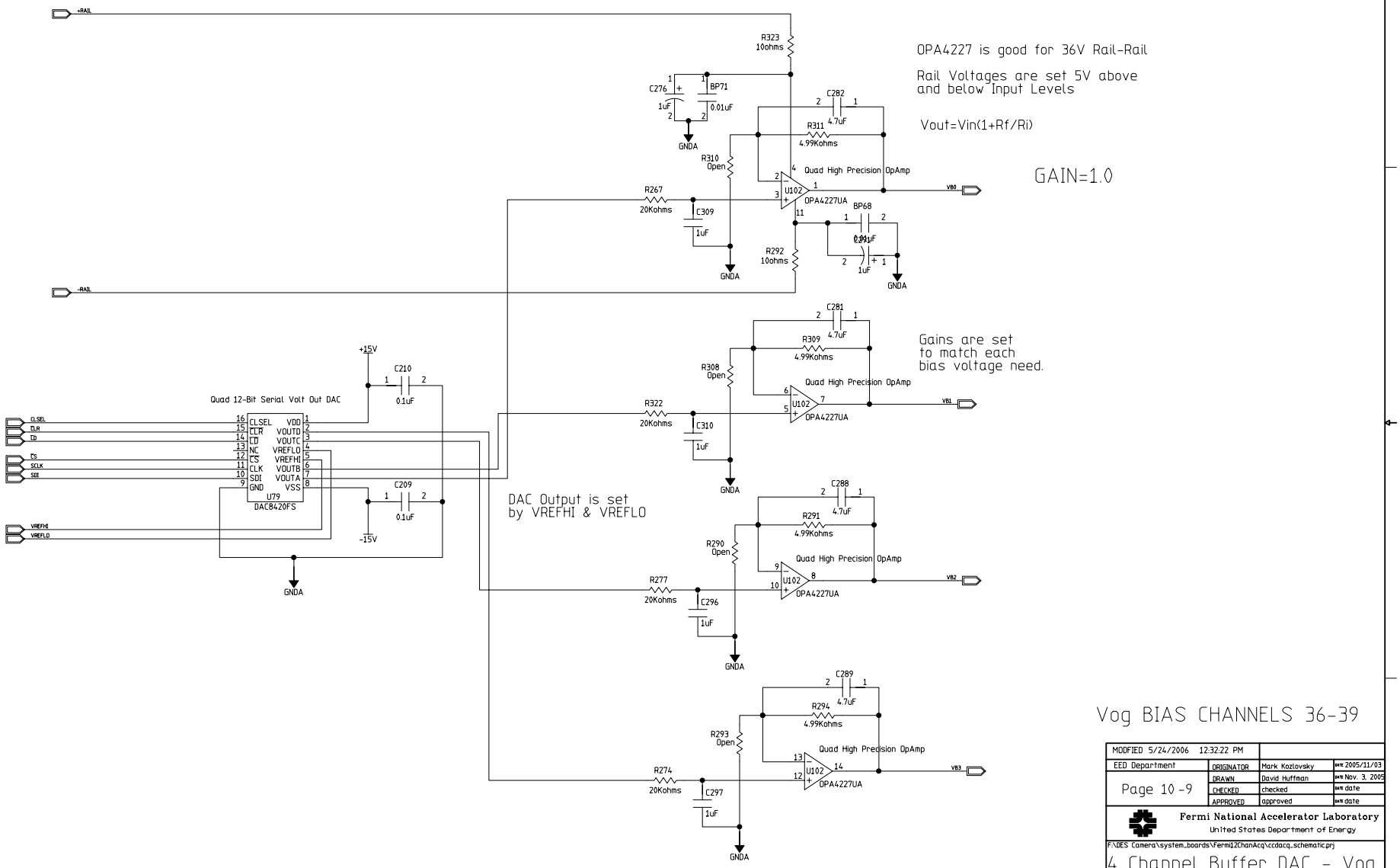
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 of 01	C



Vog BIAS CHANNELS 36-39

MODIFIED 5/24/2006 12:32:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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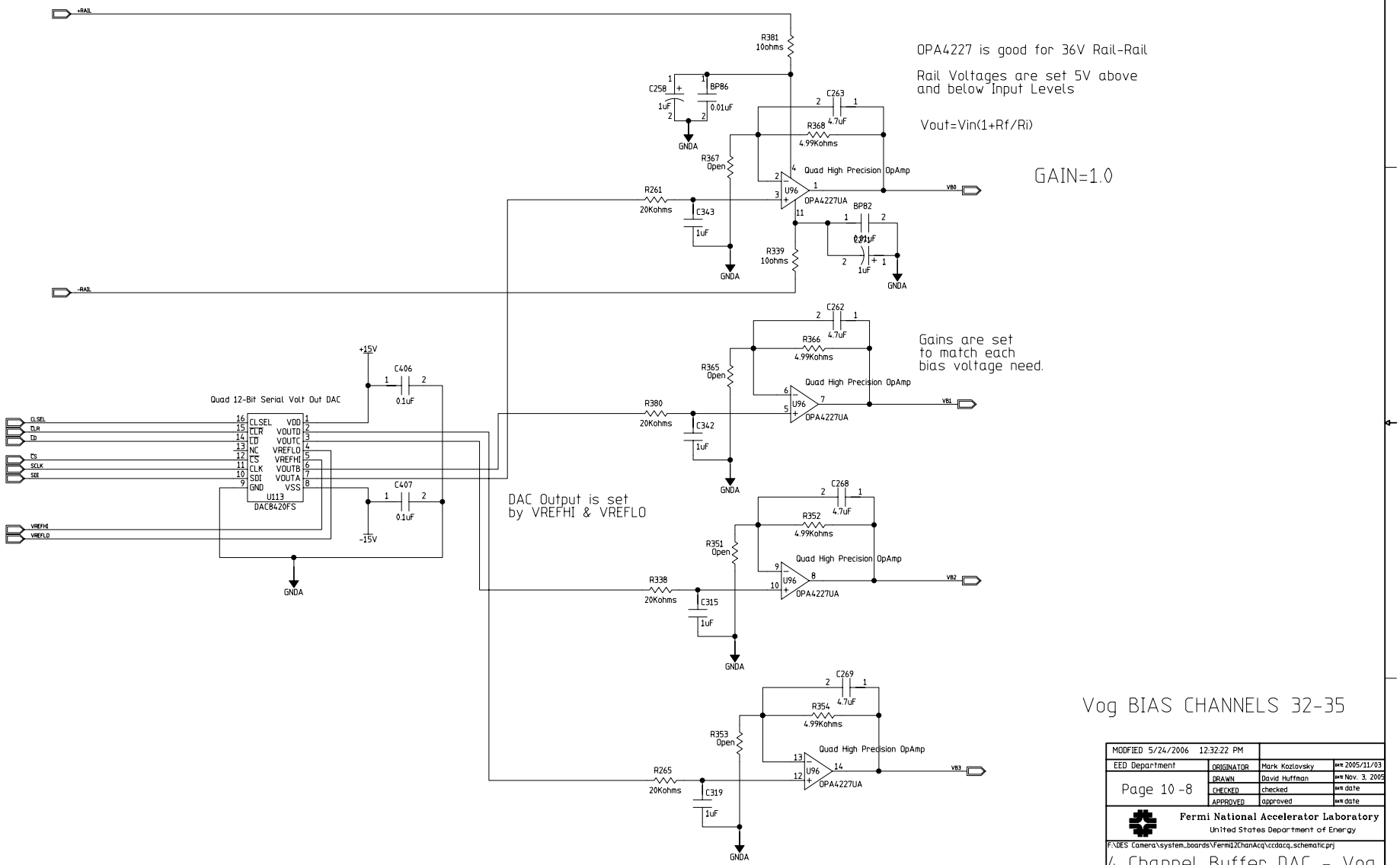
4 Channel Buffer DAC - Vog

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	173605		C


+RAIL
-RAIL
R381
10ohms
C258
1uF
BP86
0.01uF
GNDA
C263
4.7uF
R368
4.99Kohms
R367
Open
Quad High Precision OpAmp
U96
OPA4227UA
VB0
R261
20Kohms
C343
1uF
BP82
0.01uF
1uF
R339
10ohms
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above
and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1.0
C262
4.7uF
R366
4.99Kohms
R365
Open
VB1
R380
20Kohms
C342
1uF
Gains are set
to match each
bias voltage need.
+15V
C406
0.1uF
Quad 12-Bit Serial Volt Out DAC
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
U113
DAC8420FS
VDD
VOUTD
VOUTC
VREFLO
VREFHI
VOUTB
VOUTA
VSS
C407
0.1uF
-15V
DAC Output is set
by VREFHI & VREFLO
C268
4.7uF
R352
4.99Kohms
R351
Open
VB2
R338
20Kohms
C315
1uF
C269
4.7uF
R354
4.99Kohms
R353
Open
VB3
R265
20Kohms
C319
1uF
Vog BIAS CHANNELS 32-35
MODIFIED 5/24/2006 12:32:22 PM
EED Department
Page 10-8
ORIGINATOR Mark Kozlovsky date 2005/11/03
DRAWN David Huffman date Nov. 3, 2005
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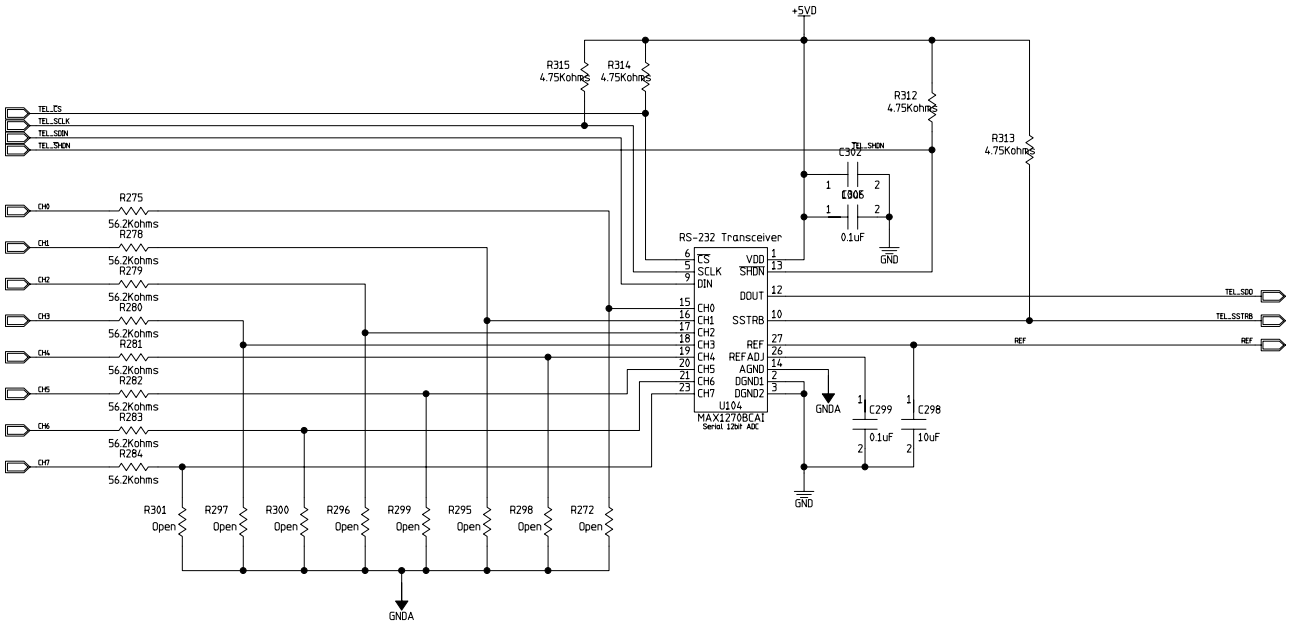
4 Channel Buffer DAC - Vog
SIZE D
DRAWING NUMBER 173605
Schematic Page 01 of 01
REV C



TELEMETRY CHANNELS BIAS 40-47

MODFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7-6	DRAWN	David Huffman	DATE Nov. 3, 2005
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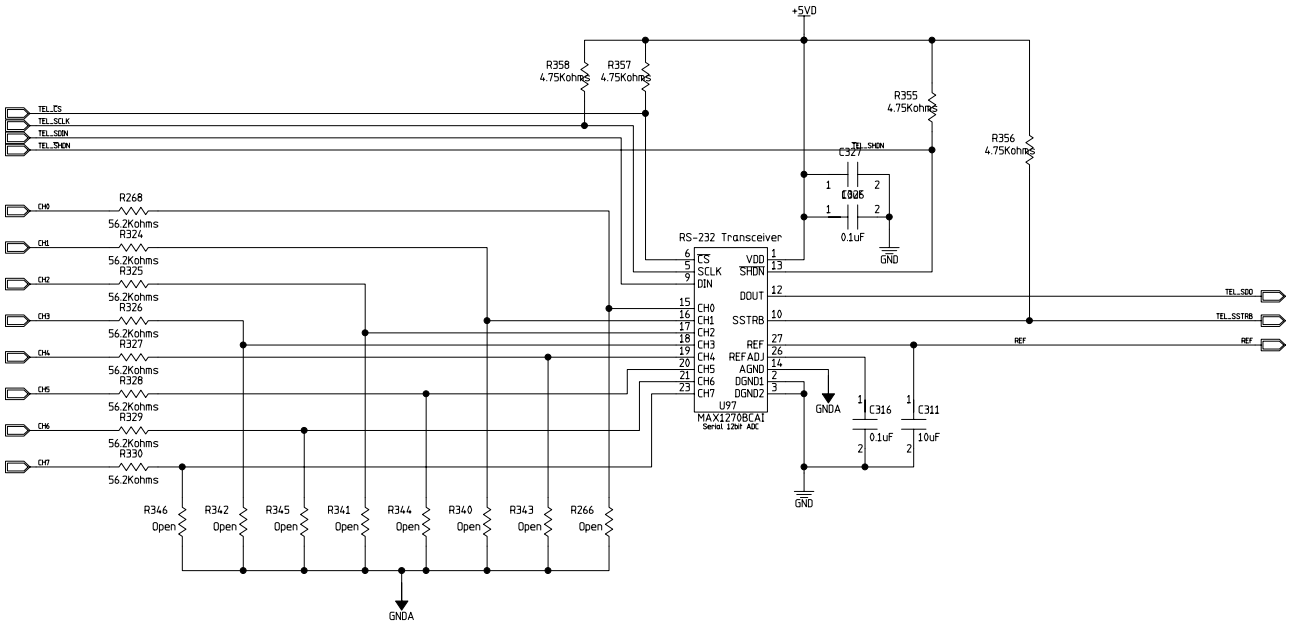
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 Of 01	C

H=BND: V=4LA



TELEMETRY CHANNELS BIAS 32-39

MODFIED 10/25/2006 3:25:22 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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	CHECKED	checked	DATE date
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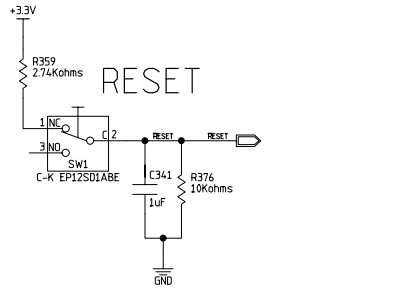
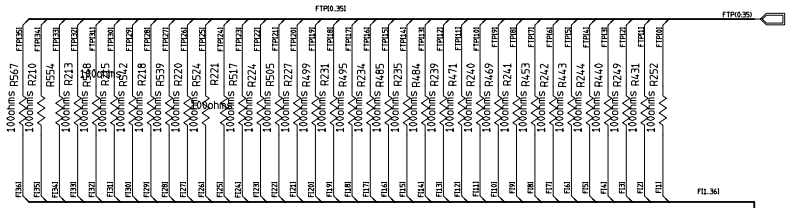
8-Channel Telemetry ADC

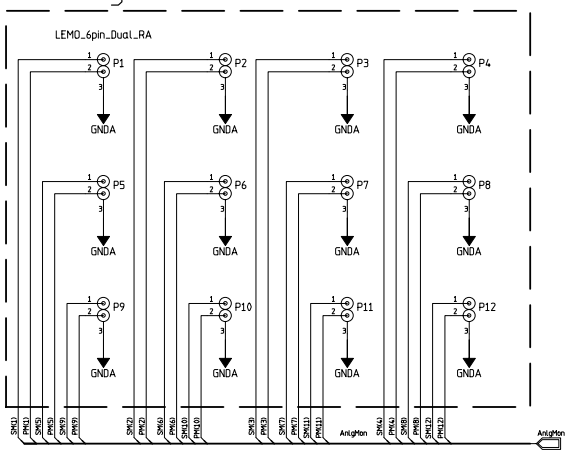
SIZE	DRAWING NUMBER		REV
D	173605	Schematic Page 01 Of 01	C

H_BND: V=4LA

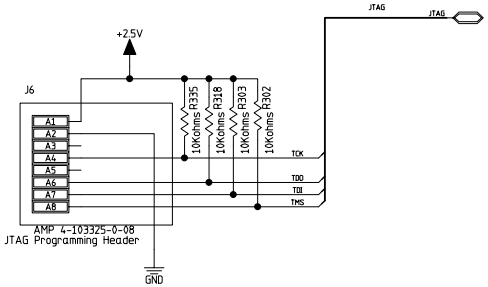




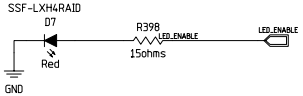
Analog Test Points



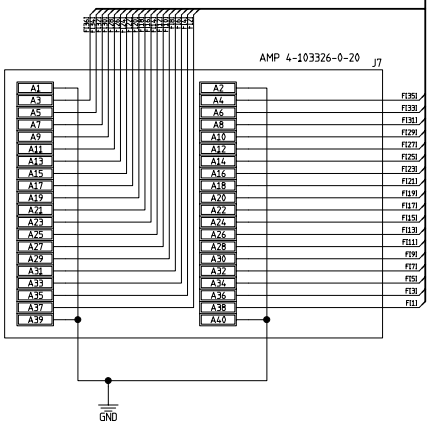
JTAG



STATUS



Digital Test Points



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EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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J6 Test Points/ Analog Mon
J7 JTAG

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H:BND: V:4LA