DARK ENERGY SURVEY

Details on CCD testing

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CCD testing and characterization

Individual CCD testing: Comparison of science requirements with performance

	LBNL CCD performance	DES requirements	
Pixel array	2048 × 4096 pixels	2048 × 4096 pixels	
Pixel size	15 μm × 15 μm	15 μm × 15 μm	
<QE (400-700 nm)>	~70%	>60%	✓ Relative QE
<QE (700-900 nm)>	~90%	>80%	✓ Relative QE
<QE (900-1000 nm)>	~60%	>50% at 1000 nm	✓ Relative QE
Full well capacity	170,000 e^-	>130,000 e^-	✓
Dark current	2 e^-/hr/pixel at –150°C	<~25 e^-/hr/pixel	✓
Persistence	Erase mechanism	Erase mechanism	✓
Read noise	7 e^- @ 250 kpix/s	< 10 e^- @ 250 kpix/sec	achieve 77%
Charge Transfer Inefficiency	$< 10^{-6}$	$<10^{-5}$	✓
Charge diffusion	6 μm	< 7 μm (*)	✓
Linearity	Better than 1%	1%	✓

✓ achieved at FNAL

Full testing for a device

- LBNL Cold probing (determines packaging priority)
- **FNAL-1 (one day)**
  - Photon transfer curve
  - Scan rails for the horizontal clocks
  - Scan rails for the vertical clocks
  - Output gate transfer curve
  - Dark current measurements
  - QE at 6 wavelengths
  - Defect counts at operating temp

  Overnight automated data taking ~600 images (22Gb)

  ⇒ report is produced after step 1 (see talk by J. Campa) (7 Terabytes)

  Automated report

- **FNAL-2 (3 days) for devices passing FNAL-1**
  - Detailed QE measurement
  - Detailed Temp studies
  - Keep cold and running to see if any problem develops
  - Package flatness

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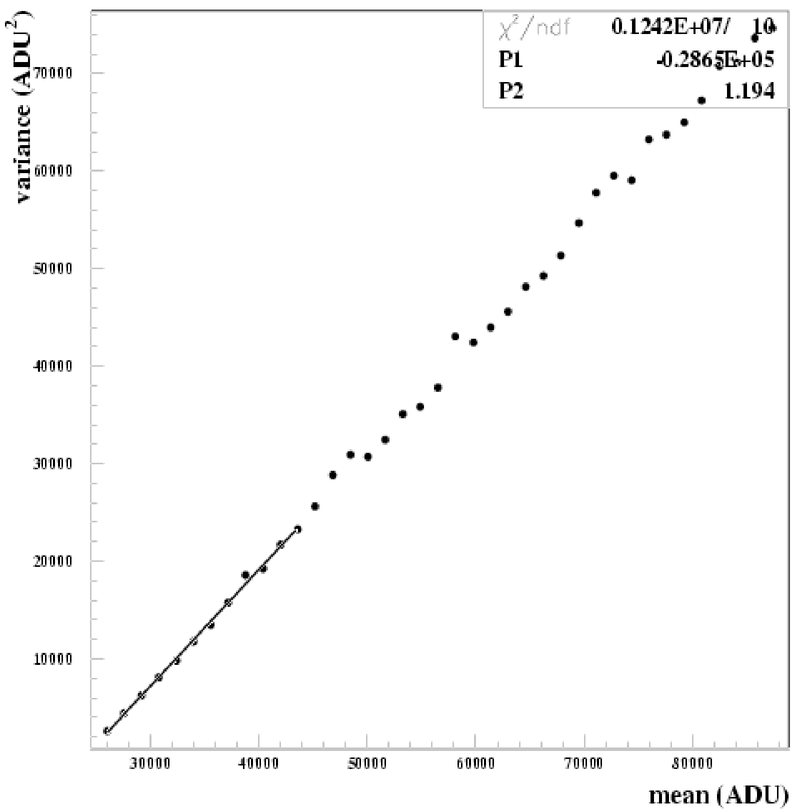
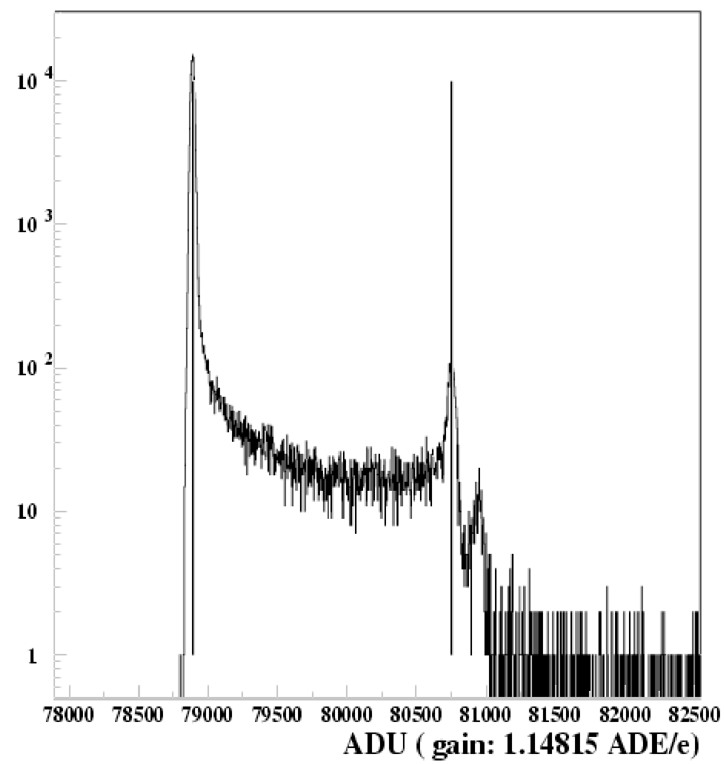
Gain determination

Conversion gain is needed to obtain the performance parameters in terms of electrons.



Assuming Poisson statistics the relation between the mean and the variance is used to determine the gain. The gain is also verified (for some devices) with Fe55 X-ray source.



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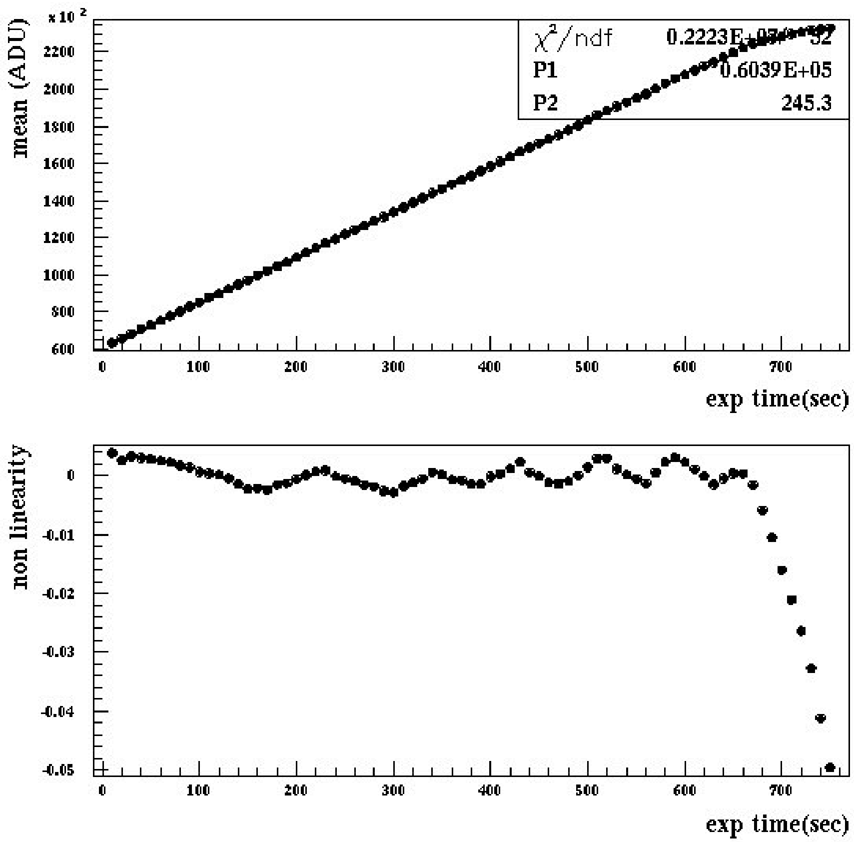
Linearity better than 1%
Full well > 130000 e



The photon transfer curve data is used to determine the linearity and full well.

In this case linearity is better than 1% up to 150000e.

requirement satisfied √

QE better >50% at 1000nm

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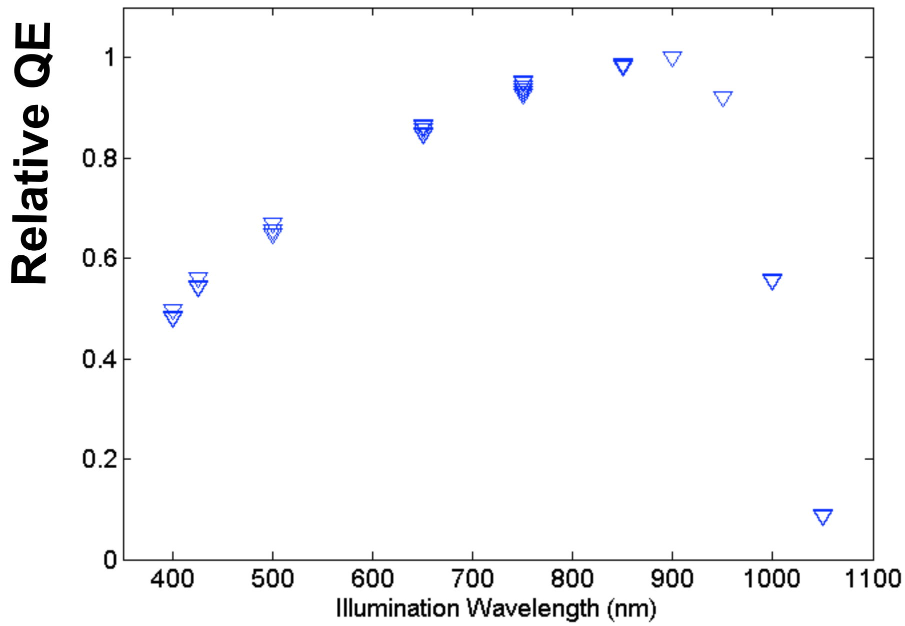

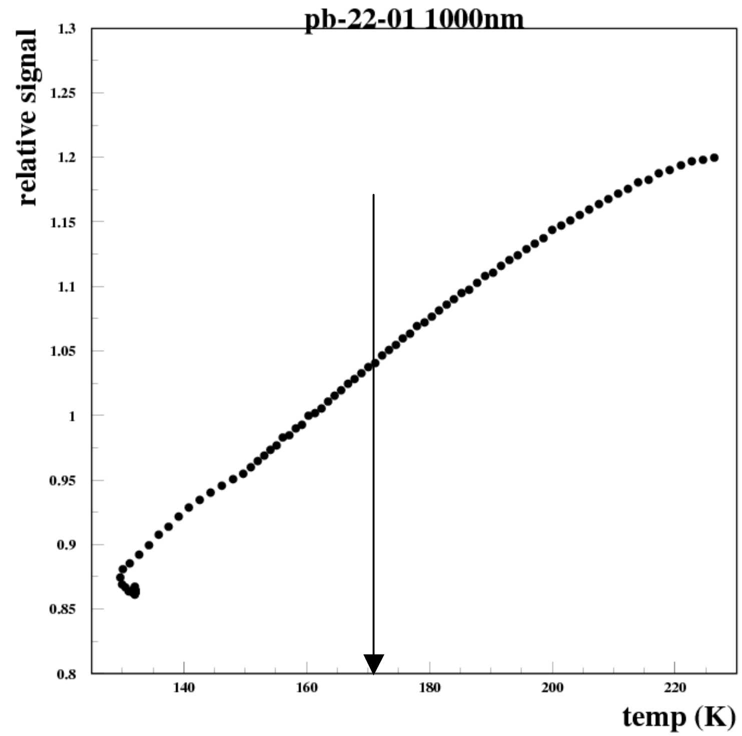

Relative QE measurements at FNAL.

Absolute QE measurement setup will be ready by the end of the summer. We are getting the expected performance.

Temp dependence for the QE in the near IR has also been studied. Operating temp T=173K.

Dark current < 25 e/pix/hour

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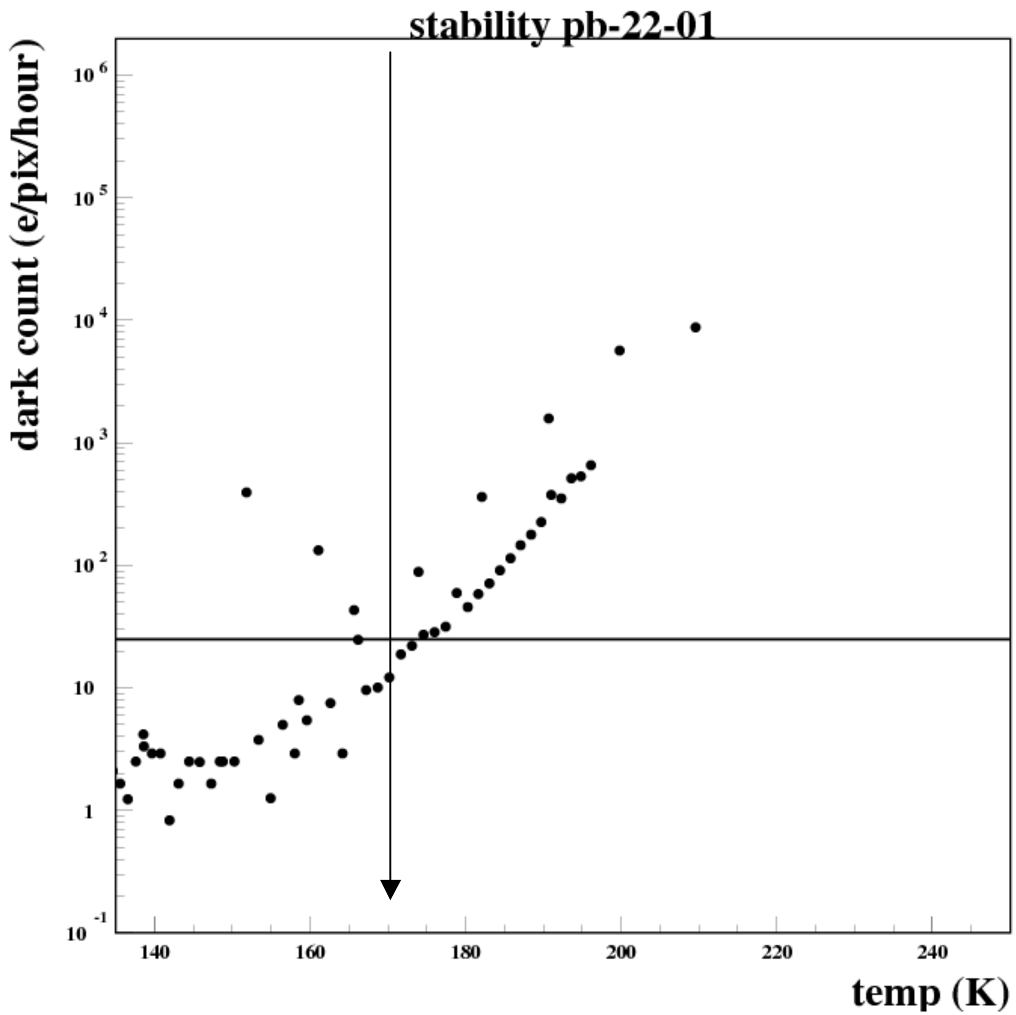
We can reach our dark current spec with our good devices.

requirement satisfied √



Voltage optimization

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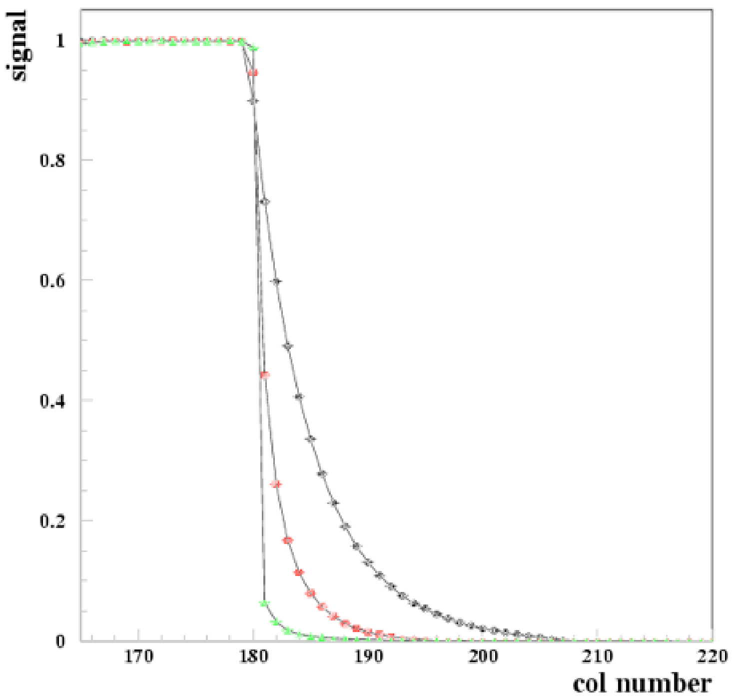
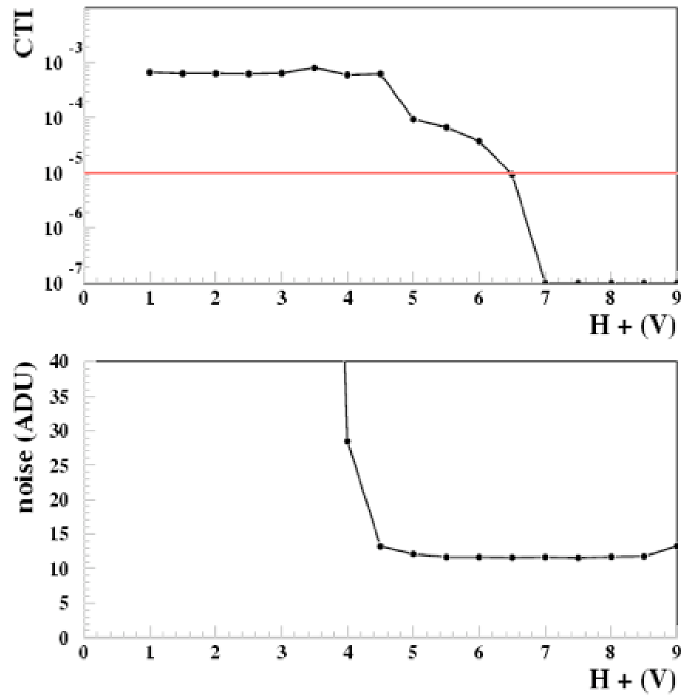
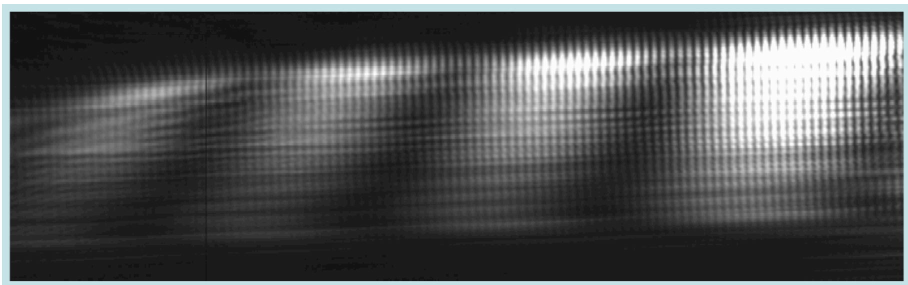


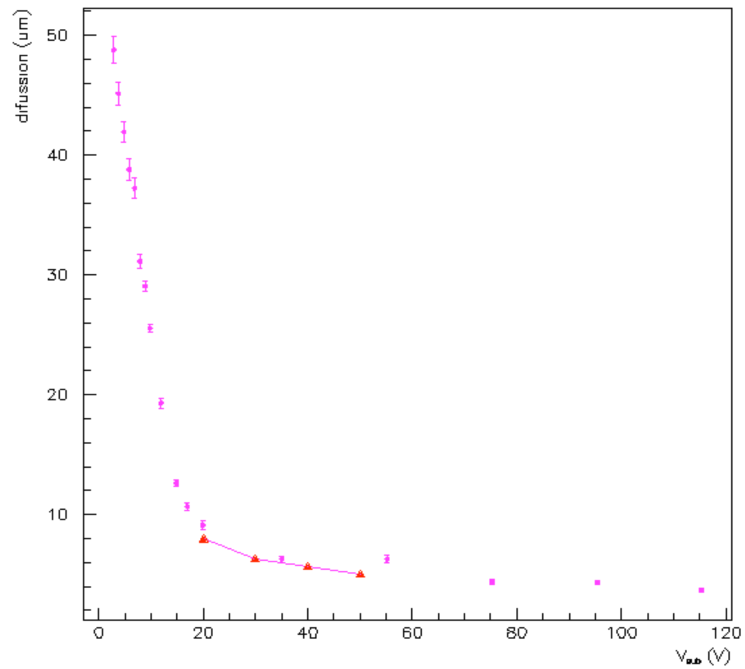


Voltage is optimized to obtain the CTE in our requirements (>0.99999).
In general this is not a problem for the DES CCDs.

The experience so far indicates that it will be possible to group devices by 3 for sharing clock settings.

Difussion < 7 μm





Using a diffraction pattern we have done measurements of diffusion that agree with our requirements, and the LBNL specs. We also expect to use the equipment at University of Michigan to confirm this measurements.

requirement satisfied √

Readout noise/speed

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Sci. Requirement: Read Noise < 10e- @ 250 kpix/sec

Best performance achieved so far:
10e @ 192 kpix/sec (pixel time of 5.2 usec)

most testing has been done @ 6.5 usec/pix

This was achieved using an amplifier on the outside of the testing dewar.
Readout time of 21sec per image, instead of the 17sec required.
Reducing the pixel time from 5.5usec to 5.2usec increased the noise from 6e to 10e.

This is a conern. The plan is to install the preamp closer to the device and continue readout time reduction studies with that hardware.

Erase mechanism speed is being studied (contributes to time between exposures)

Persistence

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Persistence can also be considered part of the readout time problem. After the device is saturated, charge gets trapped in the back surface, the trapped charge will produce extra dark current.

A way to eliminate this dark current is by driving the CCD into inversion, we can not operate in inversion mode because we have 40V in the substrate voltage (Vsub).

The idea is then to reduce the Vsub, go to inversion (V clocks high) and back to operating voltages. How fast can we do this?

We know we can do this in 10 sec or less (LBNL has done the erase in 1sec), the question is how much less. The other question is how often we need to do this.

We now have automated the ERASE mechanism in our Monsoon system (because of the 40V needed some additional hardware to do this). Soon we will know how fast we can do this.

Conclusion

- We now understand the performance of these devices, and we have the tools needed for large scale CCD testing.